# TECHNICAL HANDBOOK

# FOR

# TELEGRAPH SIGNAL GENERATOR

# TYPE TSG 40.2

THE PLESSEY COMPANY LTD
SOPERS LANE POOLE DORSET

MP MASTER
MA23737

# TECHNICAL HANDBOOK

# FOR

# TELEGRAPH SIGNAL GENERATOR

# TYPE TSG 40.2

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# AMENDMENT SHEET

| Amendment | Date | Brief Details |
| --- | --- | --- |

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

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# TELEGRAPH SIGNAL GENERATOR

# TSG 40.2

## SECTION 1 - GENERAL DESCRIPTION

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# SECTION 1

# GENERAL DESCRIPTION

## 1.1. INTRODUCTION

The Telegraph Signal Generator Type 40.2 (TSG 40.2) is a portable, general purpose telegraph test instrument providing five and eight unit code signals in the speed range from 25 bauds to 330 bauds.

Either test messages or single characters may be transmitted with a choice of stop element length and a facility for the introduction of distortion.

The equipment is a precision, solid state instrument, employing integrated circuits and discrete components. It can be used in conjunction with the Telegraph Distortion Measuring Set, Type 80.2, which is contained in an identical case. Two equipments can be mechanically joined by a rack mounting kit (Plessey Part Number 620/1/06311) when they will fit in a standard 19" rack or console.

The mains voltage selector is mounted on the rear panel, together with a tag block for making connections when the equipment is permanently installed.

All operating controls, terminals and sockets for portable operation are mounted on the front panel.

## 1.2. PHYSICAL CHARACTERISTICS

### 1.2.1. General

The integrated circuits and associated discrete components are mounted on seven printed circuit boards, interconnections being made via edge connectors which mate with sockets mounted on the chassis. Also mounted on the chassis are some discrete components and the mains supply transformer.

### 1.2.2. Dimensions

| | | |
|---|---|---|
| Width | 216mm | (8.5") |
| Height | 221mm | (8.7") |
| Depth | 406mm | (16") |
| Weight | 8.8Kg | (19.5 lbs) |
| Mains supply cable length | 2m | (6' 6") |

### 1.2.3. Environment

The equipment will operate in the range $0^{\circ}$ to + $55^{\circ}$C and can be stored in ambient temperatures from $-10^{\circ}$ to + $70^{\circ}$C.

## 1.3. ELECTRICAL CHARACTERISTICS

### 1.3.1. Signalling Speed

The signalling speed range is continuously variable from 25 to 330 bauds, with an accuracy of $\pm$ 1% overall and a resolution of 0.03 bauds. The resolution is fixed by the mechanical construction of the potentiometer.

There are two speed controls:

(a) A twelve position rotary switch, providing steps of 25 bauds, from 25 to 300 bauds.

1.3.1. Signalling Speed (Continued)

(b) A variable control from 0 to 30 bauds, with a Fine scale. One complete rotation of the knob increments by 10 bauds.

The speed is the sum of the speeds set on the switch, knob and fine scale.

The overall accuracy figure of $\pm$ 1% includes the temperature co-efficient and short term stability. The maximum change in frequency is 0.02% for 1°C change in temperature and the typical figure is 0.006% per °C.

1.3.2. Codes

Either a 5 or 8 unit code may be selected, with 1 start element and 1, 1.5 or 2 stop elements.

1.3.3. Control of Transmission

Transmission of the Test Signals may be either free running or pulsed character release.

(a) In the free running mode with the STOP/RUN switch at RUN the transmission of TEST MESSAGE or characters set by KEYS is continuous.

When the switch is set to STOP the message or character is completed before transmission is terminated.

(b) In the pulsed mode one character, i.e. from Test Message or Keys, is transmitted for each pulse.

1.3.3. Control of Transmission (Continued)

The pulses may be generated by an external equipment. The release pulses from the external equipment must be between 6 and 200V amplitude.

An internally generated pulse is obtained by operation of the STEP button, allowing manual control of pulsed transmission.

1.3.4. Test Signals

A four position rotary switch allows selection of various Test signals as follows.

1.3.4.1. Characters - Single characters, as selected by setting the KEYS (with 8 unit code operation the PARITY switch is also used), or TEST MESSAGES can be transmitted.

(a) With 5 Unit Code: Test Messages I.T.A. No. 2
See Figure 8.4.

| | | | |
|---|---|---|---|
| (i) | Long | 96 characters | FOX |
| (ii) | Medium | 32 characters | RY |
| (iii) | Short | 8 characters | Q9S |

(b) With 8 Unit Code: Test Message I.T.A. No. 5
See Figure 8.4.

| | | | |
|---|---|---|---|
| (i) | Long | 96 characters | FOX |
| (ii) | Medium | 32 characters | U* |
| (iii) | Short | 8 characters | Q9S |

1.3.4.2. Continuous MARK - A continuous MARK signal is transmitted whose polarity can be selected by the + VE/-VE MARK switch.

1.3.4.3. Continuous SPACE - A continuous SPACE signal is transmitted whose polarity is opposite to that selected by the +VE/-VE MARK switch.

1.3.4.4. 1:1 Reversals - A continuous stream of alternate MARK/SPACE signals are transmitted. These reversals cannot be distorted.

NOTE: 1:1 and 2:2 reversals can be generated by setting the CHARACTER KEYS in the appropriate manner. Distortion may be applied to reversals generated in this manner (See 5.4.6.).

1.3.5. Distortion

Various types of distortion can be applied to CHARACTERS OR TEST MESSAGES, as listed below, and is selected by a five position rotary switch, which has an OFF position.

(a) Makes each SPACE to MARK transitions occur earlier at the expense of the previous SPACE element.

(b) Makes each MARK to SPACE transitions occur earlier at the expense of the previous MARK element.

(c) Long Start element - Increases the duration of the Start element and correspondingly reduces the duration of the Stop element.

(d) Short Start element - Decreases the duration of the Start element and correspondingly increases the duration of the Stop element.

The amount of distortion is continuously variable from 0 to 50% with an overall accuracy of 1% and a resolution of $\pm$ 0.05%.

1.3.6 Output Signals

The serial output on the front and near panels is from an electronic relay capable of switching voltages from 6 to 200V, i.e. in single current mode 6V to 200V and in double current mode 6-0-6 to 100-0-100. The output current is 0 to 100mA with 250mA peak. Serial outputs at logic voltage levels are also provided on the front and rear panels.

Output data is also available in parallel form at a socket on the rear panel but this must only be used with equipments whose inputs are compatible with 74 series TTL.

1.3.7 Battery Supply

This may be provided by an external battery connected to the battery supply terminals or by an internal Battery Supply board. The following internal voltages are available.

(a) 6-0-6V at 10mA, Double current.

(b) High-0-High at 40mA, Double current.

(c) 2X + High at 40mA, Single current.

High voltages of 30V, 48V, 60V or 80V are selected by means of links on the Telegraph Battery board.

1.3.8 Mains Supply

The amplitude of mains voltage catered for is:

(a) 90 to 135V, 50 to 60 Hz, 45VA.

(b) 180 to 270V, 50 to 60 Hz, 45VA.

Further details are given in 4.2.

End of Section 1.

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

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# SECTION 2

# SYSTEM DESCRIPTION

## 2.1 INTRODUCTION

The following description is based on the Block Diagram as shown in Figure 2.1. Minimum reference is made to actual circuitry and the majority of signal paths have been shown compatible with clarity.

No power supplies are shown.

## 2.2 CHARACTER SOURCES

### 2.2.1 Introduction

There are two sources of characters:

(a) Message Generator

(b) Keys

Selection of (a) or (b) is achieved by the **CHARACTER** switch, selection of one automatically inhibits the other.

Operation can be in either 5 or 8 element mode as selected by the **STOP ELEMENT** switch.

### 2.2.2 Message Generator

The Read Only Memory (R.O.M.) stores six messages (See Figure 8.4.), three associated with 5-unit code and three with 8-unit code as follows:

(a) Long Message

(b) Medium Message

(c) Short Message

2.2.2. Message Generator (Cont'd)

The data for each character is available in parallel form, and the R.O.M. is clocked by a counter so that characters are called out sequentially.

An Optional Message Generator board is available with the same facilities as the standard Message Generator but programmed with test messages to customer requirements.

Each Message Generator includes a circuit which produces test outputs (in TTL logic level and dry contact forms) of the serial data applied to the Electronic Output board.

2.2.3. Keys

Seven Keys situated on the front panel enable the operator to select any character for transmission.

The data is available in parallel form.

In the 5-unit mode only the first five keys are used whilst in the 8-unit mode all the keys are operative in association with the ODD/EVEN parity switch.

2.2.4. Message Control

The parallel data from either the R.O.M. or Keys, as selected by the CHARACTER switch, is gated in Message Control, only one source of data being used. The STOP signal from the Interface is used to stop transmission from Message control after the Message being transmitted is completed.

The output is parallel data.

2.3. RAMP AND DISTORTION GENERATOR

2.3.1. Ramp Generation

The generator consists of a capacitor which is discharged and charged in a linear manner as shown in Figure 2.2(a).

The discharging period is constant, 30uS and coincident with this period a RESET pulse is generated.

The ramp is generated at twice Baud rate and hence two RESET pulses are generated per unit, as shown in Figure 2.2(b).

2.3.1. Ramp Generation (Cont'd)

If the Baud rate (SPEED) is altered, the rate at which the capacitor charges is changed. Figure 2.2.(c) shows the capacitor charging at a slower rate for a Speed slower than that in Figure 2.2.(a). Note that the flyback period, and hence the RESET pulses are still 30μS duration.

Adjustment of the Baud rate is controlled by:

(a) A rotary switch providing coarse control from 25 to 300 Bauds in 25 Baud increments.

(b) A three turn potentiometer continuously adjustable from 0 to 30 Bauds.

2.3.2. Distortion Generation

Distortion generation is achieved by the use of a level sensor in conjunction with the ramp.

The action is described with reference to Figure 2.3.

The amount of distortion required is set in by the DISTORTION control, a five turn potentiometer. This adjusts the level at which the level sensor switches. The selected level can be adjusted from +18V to +6V, i.e. over the complete range of the ramp.

$\overline{Sd}$ (Sense Distortion) is high when the ramp voltage is higher than the selected level, and is low when the ramp voltage is lower than the selected level.

Thus by altering the selected level the duration of $\overline{Sd}$ being high can be shortened or lengthened accordingly.

The Ramp generator is controlled by the OSC. RUN (Oscillator run) signal.

## 2.4. INTERFACE

The main function of this block is generation of the timing signals.

(a) To - The time at which transitions occur with zero distortion.

(b) Ts (T Shift) - The time at which the output of the Multiplexer is changed to the next parallel bit of the character. i.e. Assume the output from the Multiplexer is U1. At Ts this will change to U2 and so on.

(c) Td (T distortion) - The time at which transitions occur with distortion applied.

Either an ET (Early Transition) or LT (Late Transition) is selected by the DISTORTION switch.

ET is associated with:

(a) Mark Bias

(b) Short Start

LT is associated with:

(a) Space Bias

(b) Long Start

Figure 2.3. shows the waveforms with LT selected.

To is generated by gating the RESET and LT signals.

2.4. INTERFACE (Cont'd)

Ts is also the result of gating the RESET and LT signals but is produced by the negative edge of RESET.

Td is the result of gating $\overline{Sd}$ and LT.

It can be seen that To occurs during the flyback period of every second ramp, and thus occurs at Baud rate at the start of each undistorted element. Ts occurs at approximately the midpoint of an undistorted element.

The positive edge of Td can vary from To to Ts with LT selected.

Figure 2.4. shows the waveforms with ET selected.

To and Ts are again produced by gating RESET and ET signals. To is now produced by the negative edge of RESET.

The positive edge of Td can now vary from Ts to To with ET selected.

The RUN/STOP switch is used to control the generation of the timing signals.

2.5. SERIALISER

The parallel data from the Message Generator is applied to a Multiplexer which is clocked by a Counter, at either 5 level or 8 level codes as selected by the STOP ELEMENT switch.

The output of the Multiplexer is thus serial data clocked by Ts.

2.5. SERIALISER (Cont'd)

When 8-unit operation is selected a Parity Bit is required. This is inserted automatically by the Parity Generator as selected by the PARITY SW.

The serial data passes through the Data Controller clocked by To. Under control of the DISTORTION Switch, the waveform is distorted as required by Td. The Data Controller also generates the OSC RUN signal controlling the Ramp Generator.

The Serialiser Output provides a choice of:

(a) Characters - i.e. Serial data.
(b) Mark - a continuous Mark signal.
(c) Space - a continuous Space signal.
(d) 1:1 - a continuous 1:1 reversal

These are selected by the SIGNAL switch.

The output of the Serialiser is fed to the MARK POLARITY switch allowing selection of the required polarity.

2.6. TELEGRAPH BATTERY

The Telegraph Battery board produces the following supplies which are connected to drive the Electronic Output board via the SUPPLY switch:

(a) +6V/0V/-6V - connected when the supply switch is at the INTERNAL V24 position.

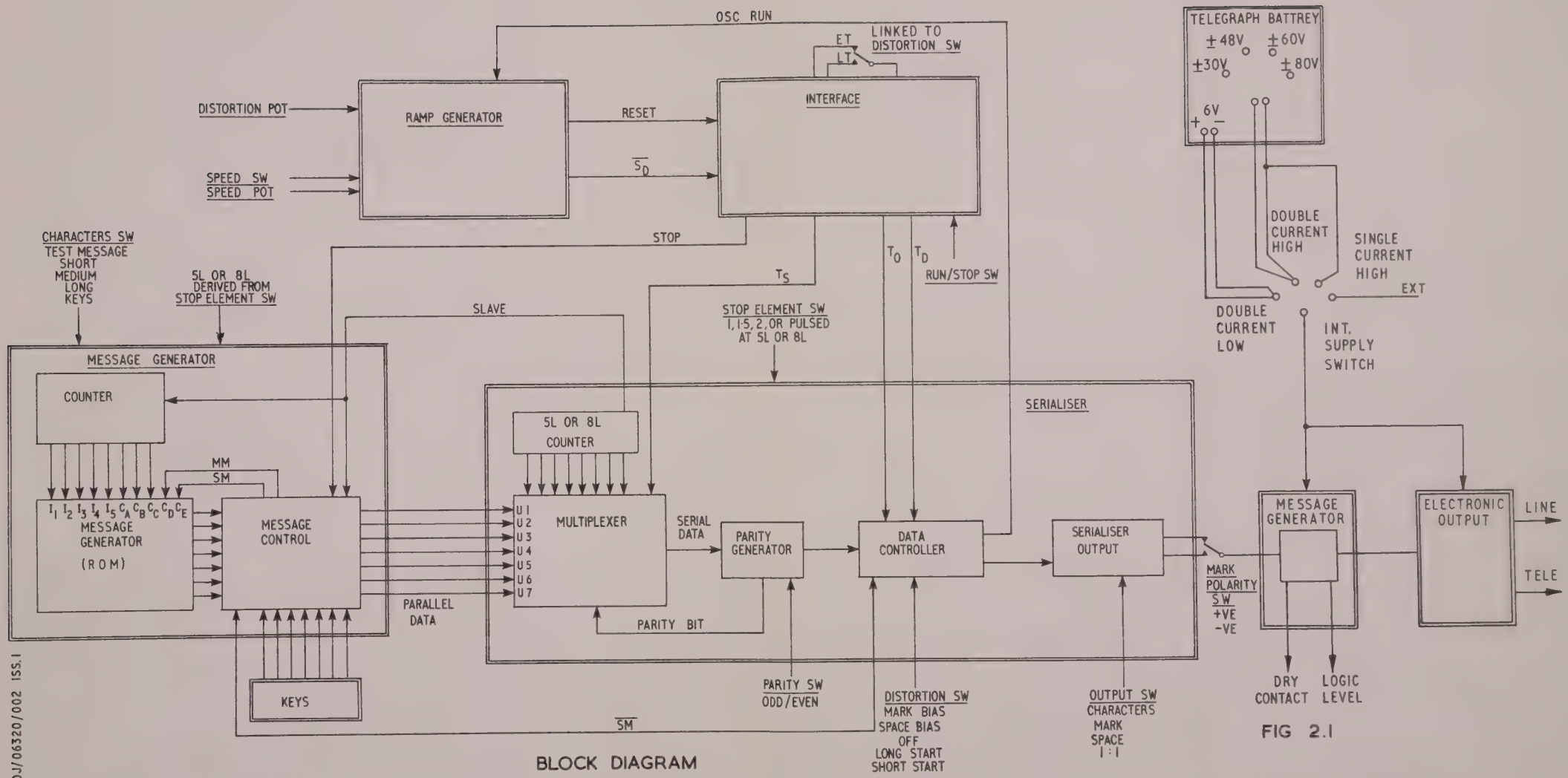
(b) +30V/0V/-30V, +48V/0V/-48V, +60V/0V/-60V or +80V/0V/-80V selected by links on the Telegraph Battery board. The selected supply is connected when the SUPPLY switch is at the INTERNAL-DOUBLE CURRENT position. Alternatively with the SUPPLY SWITCH at INTERNAL-SINGLE CURRENT position a single current version at double the selected voltage is connected, i.e. +60V/+96V/+120V/+160V.

## 2.7. ELECTRONIC OUTPUT

This is used to convert the serial data from the 0/5V logic levels to that selected by the TEL BATTERY switch.

The circuitry is the electronic equivalent of a relay contact and so the output is floating and can be tied to any voltage level within the range of the instrument.

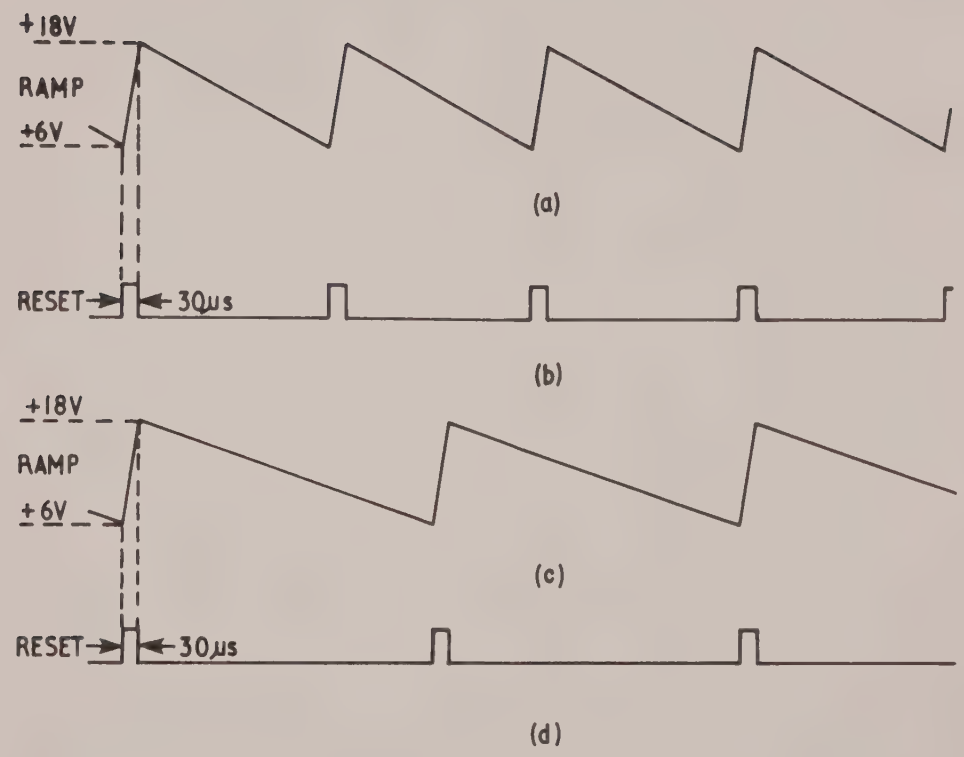
End of Section 2



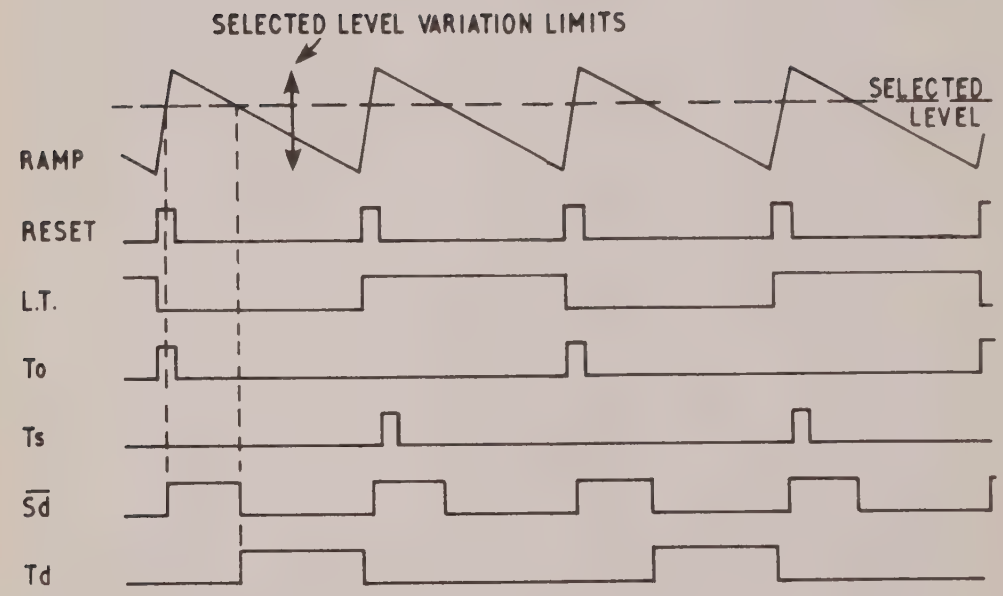

BLOCK DIAGRAM

FIG 2.1

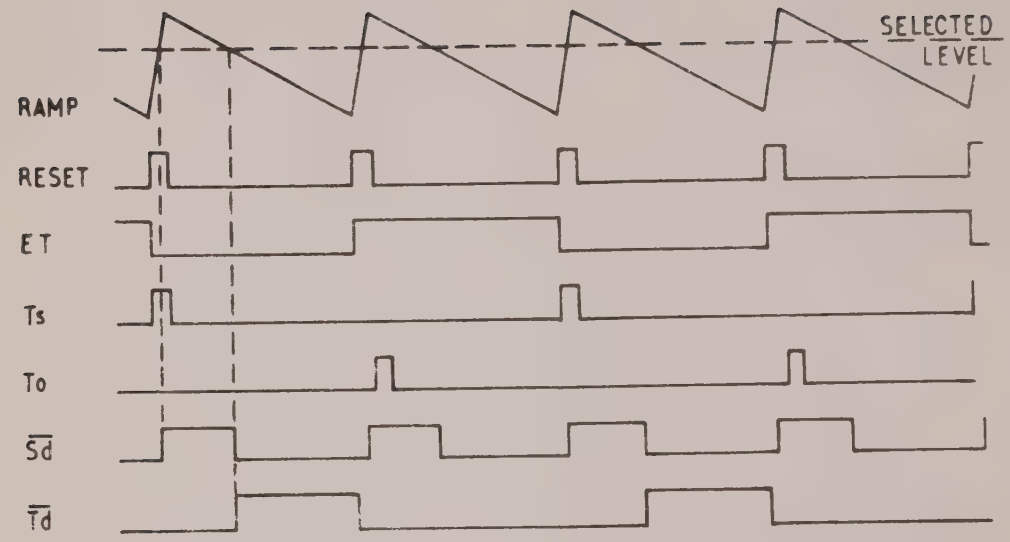
620/DJ/06320/002 ISS.1




RESET PULSE GENERATION FIG 2.2.




BASIC TIMING WAVEFORMS (L.T.) FIG. 2.3.




BASIC TIMING WAVEFORM (E.T.) FIG 2.4

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# SECTION 3

# CIRCUIT DESCRIPTIONS

## 3.1 INTEGRATED CIRCUITS

The two output levels from the TTL (Transistor Transistor Logic) elements are referred to as low and high. The corresponding voltage levels are as follows:

- Low: 0V to +0.4V, Typical +0.22V
- High: +2.4V to +5.5V, Typical +3.3V

On the logic diagrams the logic elements are identified with an IC number enabling the appropriate integrated circuit to be located on the printed circuit board. In addition the last two digits of the type reference are included for all series 74 ICs and the complete type reference for other ICs.

In the circuit descriptions of the boards, the integrated circuits are referred to using the IC number and output pin number, e.g. 1/2, IC1, output pin 2.

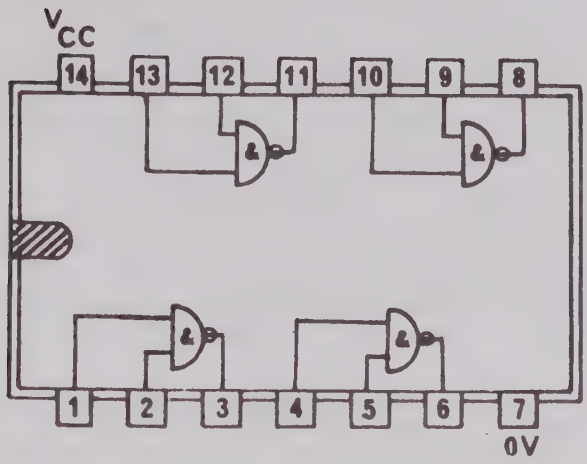
A brief description of each integrated circuit together with sketches showing the logic elements contained in each is given in the following paragraphs.

### 3.1.1 SN 7400N - Four 2-input NAND-gates

Two high inputs produce a low output (positive logic NAND) or any inpu low produces a high output (negative logic NOR).

3.1.1 SN 7400N - Four 2-input NAND-gates (Continued)

Circuit




Truth Table

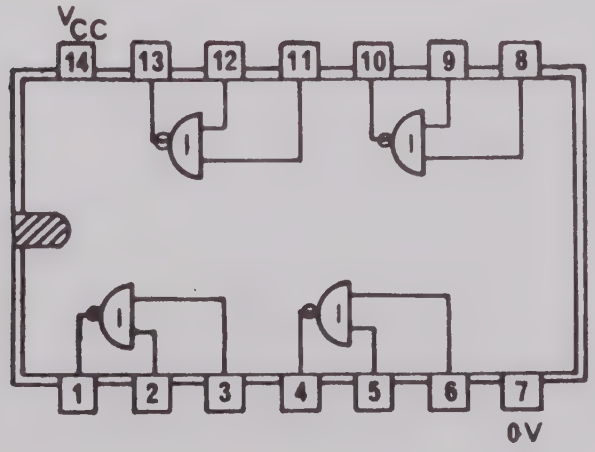
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | C |
| 0 | X | 1 |
| X | 0 | 1 |
| 1 | 1 | 0 |

X indicates that the input is irrelevant

3.1.2 SN 7402N - Four 2-input Nor-gates

Either input high produces a low output (positive logic NOR) or both inputs low produces a high output (negative logic NAND).

Circuit



3.1.2 SN 7402N - Four 2-input Nor-gates (Continued)

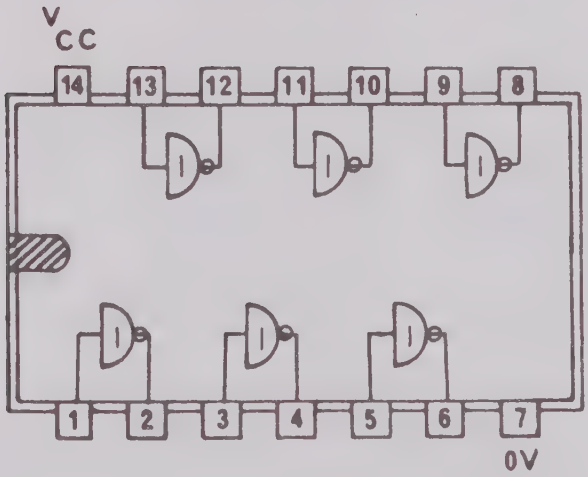
Truth Table

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | C |
| 0 | 0 | 1 |
| 1 | X | 0 |
| X | 1 | 0 |

X indicates that the condition of the input is irrelevant

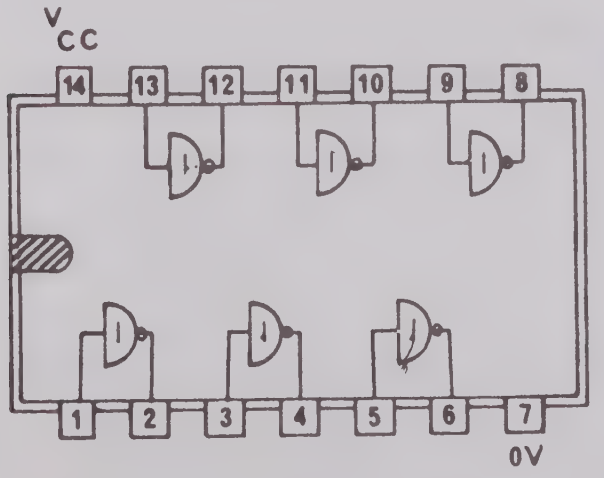
3.1.3 SN 7404N - Six Inverters

Invert the voltage level of the input signal.



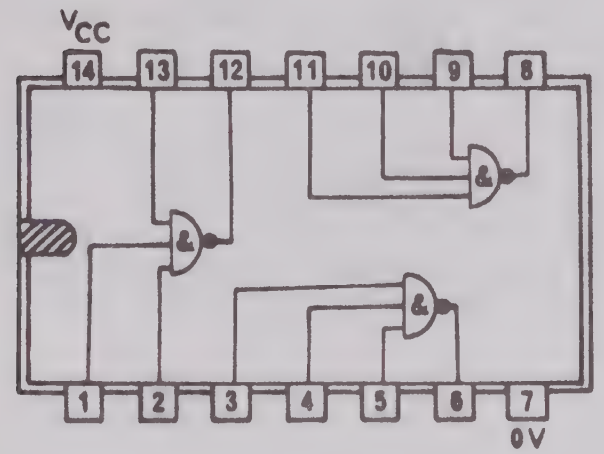

3.1.4 SN 7406N - Six Inverter/Buffer Drivers

Invert the voltage level of the input signal.



### 3.1.5 SN 7410N - Three 3-Input NAND-gates

Three high inputs produce a low output (positive NAND) or any input low produces a high output (negative NOR).




Truth Table

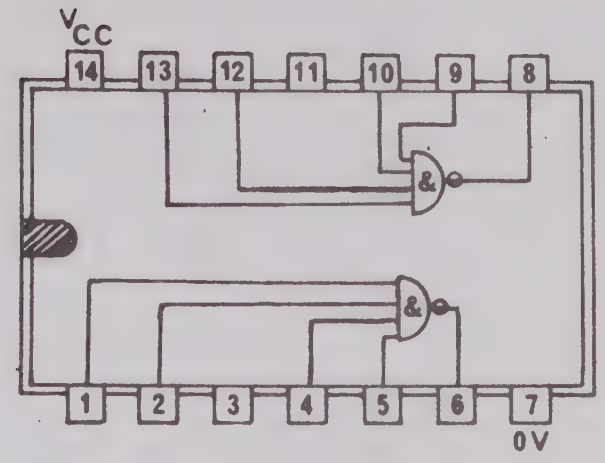
| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | D |
| X | X | 0 | 1 |
| X | 0 | X | 1 |
| 0 | X | X | 1 |
| 1 | 1 | 1 | 0 |

X indicates that the condition of the input is irrelevant

### 3.1.6 SN 7420N - Two 4-input NAND-gates

Four high inputs produces a low output (positive NAND) or any input low produces a high output (negative NOR).

3.1.6 SN 7420N - Two 4-input NAND-gates (Continued)



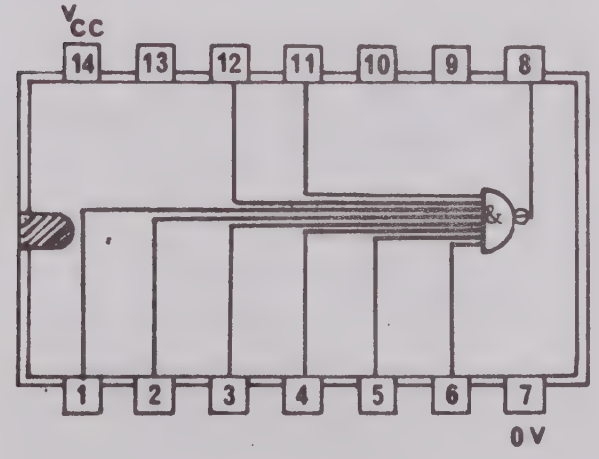

Truth Table

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | E |
| 0 | X | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

X indicates that the condition of the input is irrelevant

3.1.7 SN 7430N - One 8-input NAND-gate

Eight inputs high produces a low output (positive NAND), any input low produces a high output (negative NOR).



3.1.7 SN 7430N - One 8-input NAND-gate (Continued)

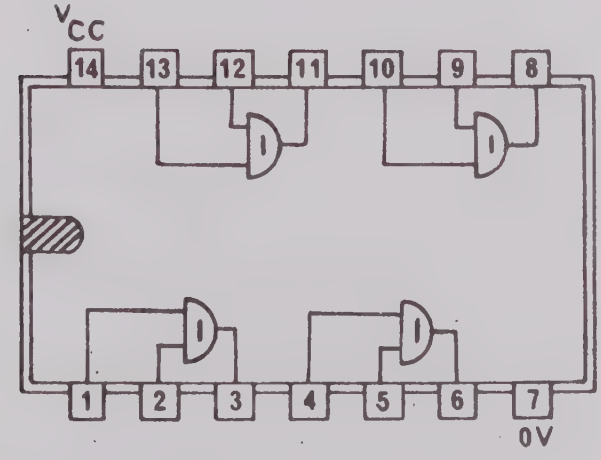
Truth Table

| INPUTS | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | Y |
| 0 | X | X | X | X | X | X | X | 1 |
| X | 0 | X | X | X | X | X | X | 1 |
| X | X | 0 | X | X | X | X | X | 1 |
| X | X | X | 0 | X | X | X | X | 1 |
| X | X | X | X | 0 | X | X | X | 1 |
| X | X | X | X | X | 0 | X | X | 1 |
| X | X | X | X | X | X | 0 | X | 1 |
| X | X | X | X | X | X | X | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

X indicates that the condition of the input is irrelevant

3.1.8 SN 7432N - Four 2-input OR-gates

Any input high produces a high output (positive OR), both inputs low produce a low output (negative AND).



3.1.8 SN 7432N - Four 2-input OR-gates (Continued)

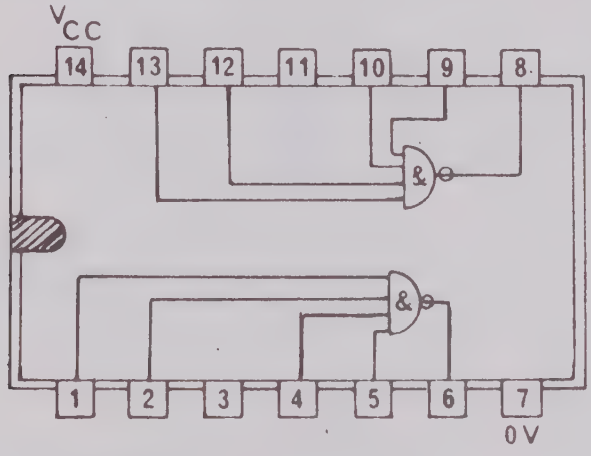
Truth Table

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | C |
| 0 | 0 | 0 |
| 1 | X | 1 |
| X | 1 | 1 |

X indicates that the condition of the input is irrelevant

3.1.9 SN 7440N - Two 4-input NAND-gate Buffers

Four inputs high produces a low output (positive logic NAND) or any input low produces a high output (negative logic NOR).




Truth Table

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | $\overline{E}$ |
| 0 | X | X | X | 1 |
| X | 0 | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

X indicates that the condition of the input is irrelevant

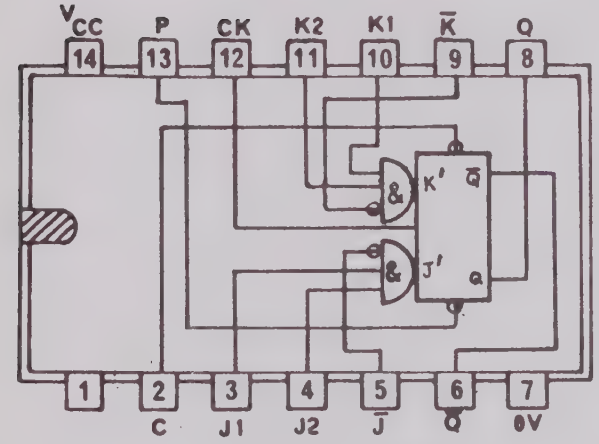
3.1.10 SN 7470N - One Edge Triggered JK Bistable

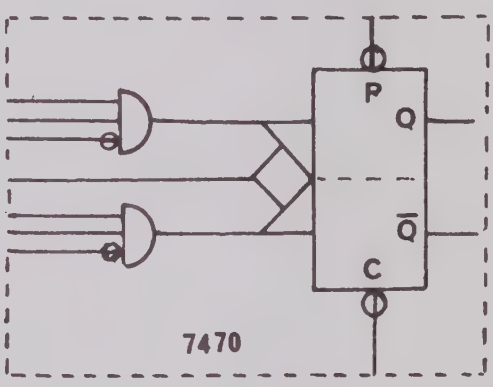
The clock pulse is directly connected and the bistable is clocked on the positive going edge.

(a) With CLEAR low bistable is clamped in the reset state ($\overline{Q}$ - high, Q - low).

(b) With PRESET low bistable is clamped in the set state (Q - high, $\overline{Q}$ - low).

(c) If PRESET and CLEAR are high the information on the inputs is clocked into the bistable by the clock pulse.




Truth Table

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| PRESET | CLEAR | CLOCK | J' | K' | Q | $\overline{Q}$ |
| 0 | 1 | X | X | X | 1 | 0 |
| 1 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | X | X | X | Unstable state (both high) | |
| 1 | 1 | ↑ | 0 | 0 | No change | |
| 1 | 1 | ↑ | 1 | 0 | 1 | 0 |
| 1 | 1 | ↑ | 0 | 1 | 0 | 1 |
| 1 | 1 | ↑ | 1 | 1 | Changes state | |
| 1 | 1 | 0 | X | X | No change | |

X indicates that the condition of the input is irrelevant

3.1.11 SN 7472N - One Master Slave JK Bistable

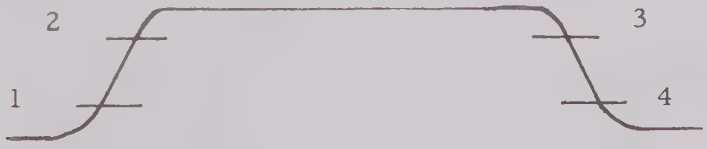
The circuit operates as follows:

(a) With CLEAR low the bistable is clamped in the reset state ($\overline{Q}$ - high, Q - low).

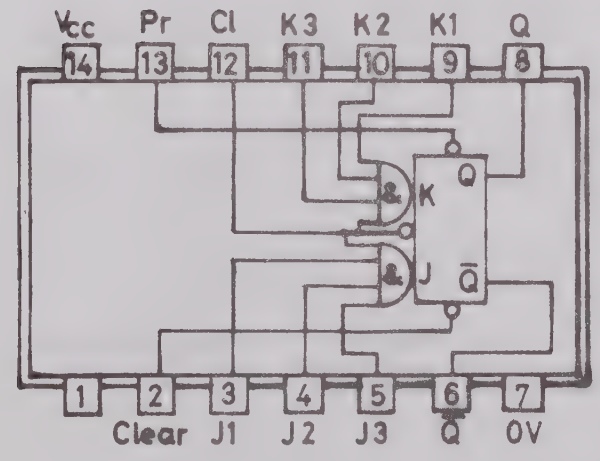
(b) With PRESET low the bistable is clamped in the set state (Q - high, $\overline{Q}$ - low).

(c) If CLEAR and PRESET are both high, the data applied to the J and K inputs is switched into the bistable under control of the clock pulse. The resultant outputs following the clock sequence are given in the truth table.

The sequence of transferring data under control of the clock pulse is as follows:




1. J and K isolated from Q and $\overline{Q}$.
2. Data applied to J and K.
3. J and K disconnected from inputs.
4. Q and $\overline{Q}$ outputs change according to JK inputs (see truth table).



3.1.11 SN 7472N - One Master Slave JK Bistable (Continued)

Truth Table

| Time 2 | | Time 4 |
|---|---|---|
| J | K | Q |
| 0 | 0 | No change |
| 0 | 1 | 0 (Low) |
| 1 | 0 | 1 (High) |
| 1 | 1 | Changes state |

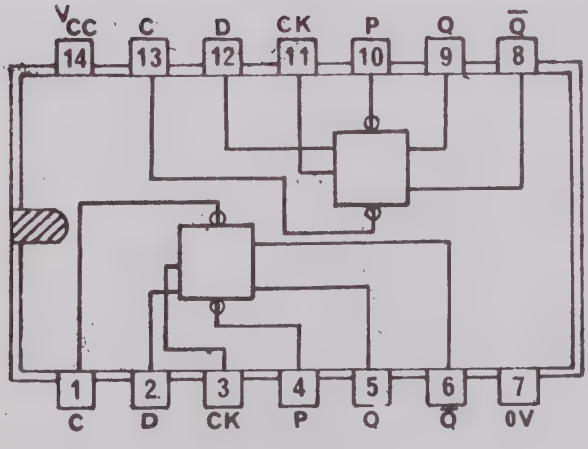
3.1.12 SN 7474N - Two D-Type Edge Triggered Bistables

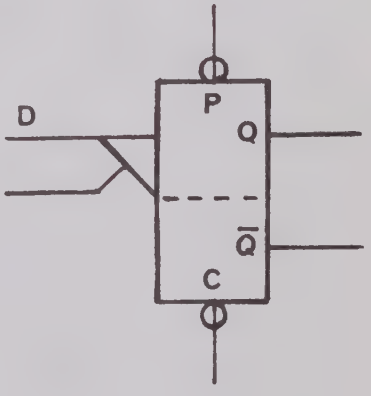
Each bistable operates as follows:

(a) With CLEAR (C) low the bistable is clamped in the next state ($\bar{Q}$ - high, Q - low).

(b) With PRESET (P) low the bistable is clamped in the set state (Q - high, $\bar{Q}$ low).

(c) With CLEAR and PRESET both high information at DATA (D) is transferred to Q on the high going edge of the clock pulse.



3.1.12 SN 7474N - Two D-Type Edge Triggered Bistables (Continued)

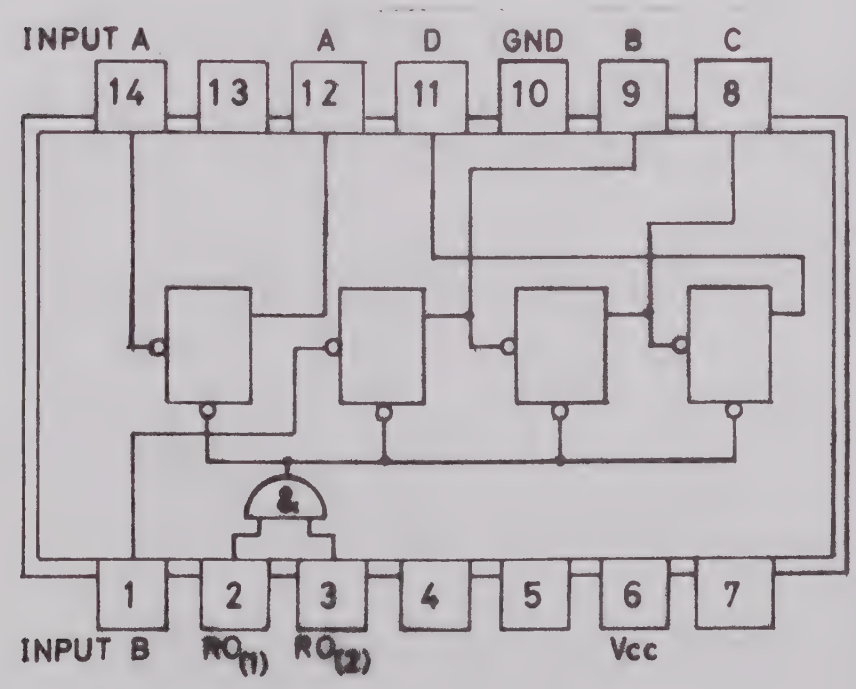
Truth Table

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| PRESET | CLEAR | CLOCK | D | Q | $\overline{Q}$ |
| 0 | 1 | X | X | 1 | 0 |
| 1 | 0 | X | X | 0 | 1 |
| 0 | 0 | X | X | 1 (Unstable state) | 1 |
| 1 | 1 | ↑ | 1 | 1 | 0 |
| 1 | 1 | ↑ | 0 | 0 | 1 |
| 1 | 1 | 0 | X | No change | |

X indicates that the condition of the input is irrelevant

3.1.13 SN 7493AN - One 4-bit Binary Counter

This includes four negative edge triggered bistables which may be used as a 4-bit counter by applying the clock signal to input A and connecting output A to input B. Alternatively the element may be used as a 3-bit counter with the other bistable used independently. The bistables are clamped in the reset state by applying high signals to inputs $RO_{(1)}$ and $RO_{(2)}$.



3.1.13 SN 7493AN - One 4-bit Binary Counter (Continued)

Truth Table (4-bit operation)

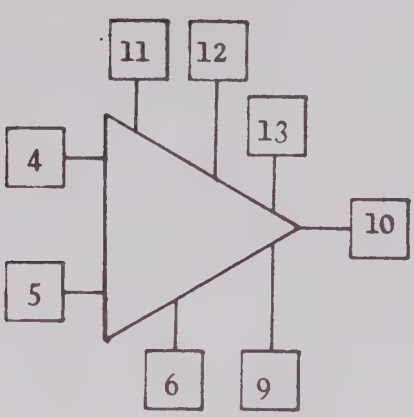
| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | D | C | B | A |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

3.1.14 SN 72709N - Operational Amplifier

The 72709 is a high gain amplifier featuring a high input impedance, low input offset voltages and currents, and a high output swing capability.

Details of connections for N-Pack (14L - D.I.L.) are shown as follows.

3.1.14 SN 72709N - Operational Amplifier (Continued)

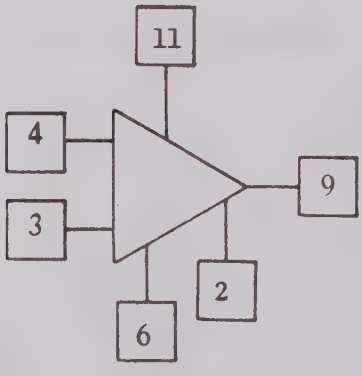



1. NC.
2. NC.
3. Input Frequency Compensation B.
4. Inverting Input.
5. Non Inverting Input.
6. Vcc - (0v)
7. NC.
8. NC.
9. Output Frequency Compensation.
10. Output.
11. Vcc + (+24V).
12. Input Frequency Compensation A.
13. NC.
14. NC.

3.1.15 SN 72710N - Comparator

The 72710 is a high speed voltage comparator with a differential input and a low impedance output. It features low offset and drift characteristics, making it suitable for establishing switching points on a voltage waveform, with a high accuracy over a wide temperature range.

Details of the N Pack connections are shown below.

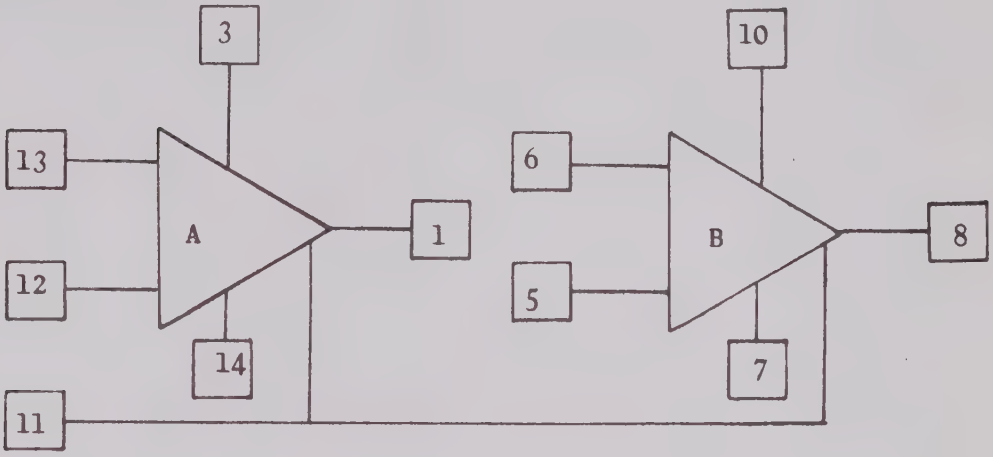



1. NC.
2. GND (+ 12V).
3. Non-inverting input.
4. Inverting input.
5. NC.
6. 6 $Vcc_2$ (+6V).
7. NC.
8. NC.
9. Output.
10. NC.
11. $Vcc_1$ (+24V).
12. NC.
13. NC.
14. NC.

Note: The voltage levels shown are those actually used in the TSG 40.2.

### 3.1.16 SN 72720N - Comparators

The SN 72770N contains two 72710N circuits.

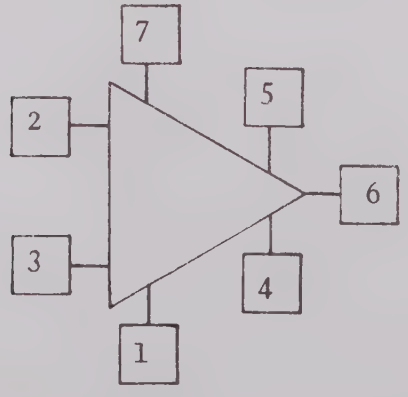



1. Output Amp A.
2. NC.
3. Vcc + (+24V) Amp A.
4. NC.
5. Non inverting Input - Amp B.
6. Inverting Input - Amp B.
7. Vcc - (+6V) Amp B.
8. Output Amp B.
9. NC.
10. Vcc + (+24V) Amp B.
11. GND (+12V).
12. Non inverting Input - Amp A.
13. Inverting Input - Amp A.
14. Vcc - (+6V) Amp A.

Note: The voltage levels shown are those actually used in the TSG 40.2.

### 3.1.17 SN 72741P - Operational Amplifier

The 72741 is a high performance amplifier which can be used in a wide range of analogue applications.




1. Offset Null.
2. Inverting Input.
3. Non Inverting Input.
4. -V.
5. Offset Null.
6. Output.
7. +V.
8. NC.

3.1.18 Brief IC Specifications

| | |
|---|---|
| Temperature Range: | $0^{\circ}C$ to $70^{\circ}C$. |
| Supply Voltage Vcc: | +4.75V to +5.25V. |
| Output Levels: | Low - 0 to +0.4V. |
| | High - +2.4 to +5.5V. |

3.2 MAINS SUPPLY INPUT (Figure 8.6)

The mains input is controlled by the mains SUPPLY switch S14. A red indicator lamp ILP1 is illuminated when the supply is ON. The MAINS SELECTOR, VS1 allows two input ranges to be selected together with the appropriate fuse. Other ranges may be obtained by altering transformer tappings as shown in the table below.

| TAPPING POINTS | RANGE | |
|---|---|---|
| | With VS1 set to 195 - 225 | With VS1 set to 97 - 127 |
| C and G | 180 - 240 | 90 - 120 |
| B and F | 195 - 255 | 97 - 127 |
| A and E | 210 - 270 | 105 - 135 |

When the equipment leaves the factory, tapping points B and F are connected.

T1 provides:

(a) 192V r.m.s. centre tapped.

(b) 38V r.m.s.

(c) 9V r.m.s.

(d) 22V r.m.s. centre-tapped.

## 3.3 TELEGRAPH BATTERY (Figures 7.1 and 8.7)

### 3.3.1 General

The Telegraph Battery output (or a supply from an External Battery, as selected by the OUTPUT SUPPLY switch, S17,) is switched to the transmission line by the Electronic Output board. The signals thus switched define the MARK and SPACE voltage levels. The outputs of S17 are protected by FS3 and FS4 (Figure 8.6).

### 3.3.2 Function

The function of the Telegraph Battery is to provide the following supplies:

(a) ± 6V d.c. - Low voltage supply.

(b) ± 30V d.c.
(c) ± 48 d.c.
(d) ± 60V d.c.
(e) ± 80V d.c.
- High voltage selected by links.

The supplies are produced from a rectified a.c. supply which is applied to a Zener diode potential divider chain. Preselection of the required high supply is by means of links A and B on the Telegraph Battery PCB (see Figure 8.7).

The Telegraph Battery is normally used for Double Current operation, (signal voltage levels for MARK and SPACE are of opposite polarities and of equal amplitude about TEL.E.).

### 3.3.3 Operation

The 192V a.c. supply between pins 5 and 6 is full wave rectified by diodes D1 to D4 and smoothed by reservoir capacitors C1 and C2. Current overload protection for the mains transformer is provided by FS1 and FS2.

TR1 and TR2 are constant current drains for the Zener diode potential divider chains. The bases of the two transistors are held at 4.3 volts by D10 and D14. R5 and R6 are shunts to D8, D9 and D7, D6 enabling these diodes to be low power components.

3.3.3 Operation (Continued)

The outputs at pins 11 and 10 must be symmetrical about pin 22, TEL.E. To achieve this balance provision is made for shorting out some Zener diodes. The balancing procedure is given in 6.9.

Selection of the required high voltage output is simply a matter of connecting links A and B in the appropriate positions.

## 3.4 POWER SUPPLY UNIT (Figures 7.3 and 8.8)

### 3.4.1 Introduction

The a.c. voltages from which the d.c. supplies are derived are fed from the mains transformer T1. The d.c. output voltages are:

(a) +24V D.C.

(b) +5V D.C.

(c) -4V D.C.

Components which are mounted on the chassis and shown in Figure 8.6 have also been included in Figure 8.8 to facilitate description of the operation.

### 3.4.2 +24 Volt Supply

The 38V a.c. input at pins 6 and 9 is rectified by the full wave bridge D2/3/4/5 and the reservoir capacitor C1 mounted on the chassis provides smoothing.

Current overload protection is provided by FS1.

The stabiliser is a conventional series regulator circuit.

The output voltage is monitored by the emitter-coupled pair amplifier TR1/TR2 and compared with the stable reference voltage 5.6V provided by D1.

Should the output voltage of the stabiliser increase, TR2 collector current increases producing a corresponding increase in the collector currents of TR3 and TR4. This causes the base bias voltage on TR5 and series stabiliser TR1 to reduce thus reducing the stabiliser output voltage by an amount approaching the original increase. The mechanism works in reverse for an initial reduction in output voltage.

The method of regulation is a continuous feedback process which produces an output voltage which is almost unaffected by changes in working voltage within its range. R1 enables the output voltage to be finely adjusted.

### 3.4.3 +5 Volt Supply

The rectification and stabilisation circuit is similar in concept to the +24 Volt system. R17 provides fine adjustment of the output voltage.

### 3.4.4 Over Voltage Protection

The +5V supply provides power for all digital integrated circuits in the system. The maximum voltage which may be applied to these devices is +7V. It is therefore essential that a fault in the power unit should not allow the voltage to exceed this limit. This is achieved by using a thyristor CSR1 which conducts when the output voltage of the +5V supply exceeds +6.3V, and blows the fuse FS2.

### 3.4.5 -4 Volt Supply

The 22V centre-tapped winding of T1 feeds pins 35 and 36 of the Power Supply board. Rectifier D13/D14 produce a full wave rectified d.c. voltage. C5 the reservoir voltage which is applied to the capacitor provides smoothing and the voltage is applied to D12 which develops a stable 4 volts which is routed to pin 38 of the board.

## 3.5 RAMP AND DISTORTION GENERATOR (Figure 7.2. and 8.9)

### 3.5.1 Introduction

This board generates the timing signals used in the system and also provides the means for controlling distortion. The following circuits are provided on the board:

(a) Ramp generator.

(b) Distortion Generator.

(c) Bauds monitor.

### 3.5.2 Ramp Generator

There are two modes in which the ramp may be operated:

(a) Continuous (Normal Mode).

(b) Intermittent (Pulse Mode).

The basis of the ramp generator is the charging of a capacitor from a current source, in order to achieve a linear relationship between voltage and time. This is implemented by using an integrator technique, which has the added advantage of providing long time constants using a relatively small value of capacitance.

A simplified diagram of the ramp generator appears in Figure 3.1.

In the Normal Mode edge connector pin 31 is held high and pin 29 low.

TR4 is held switched off, allowing C6 to charge and discharge as necessary.

#### 3.5.2.1 Comparator Operation

Consider IC2a, the voltage on pin 12 is held at +12V. When the voltage on pin 13 is less than +12V the output at 2/1 is high. Similarly when the voltage on pin 13 is greater than +12V the output at 2/1 is low, i.e.

Pin 13 $<$ +12V  Pin 1 high.

Pin 13 $>$ +12V  Pin 1 low.

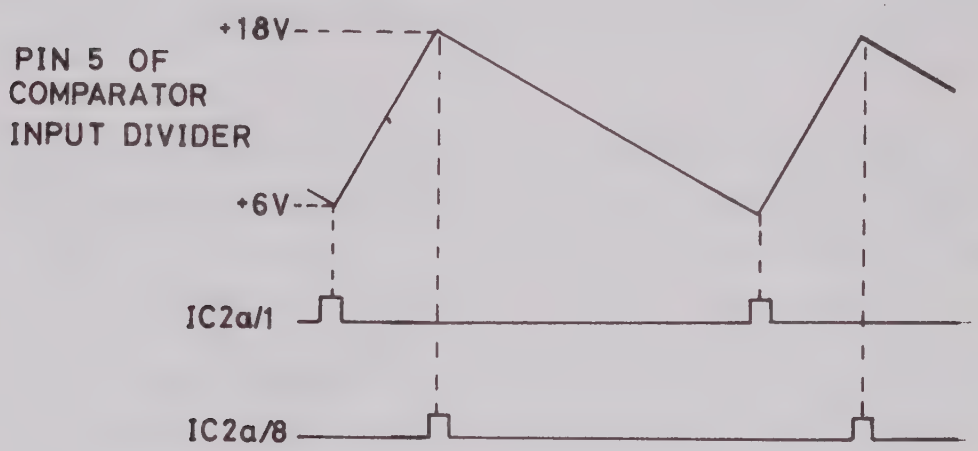
3.5.2.1 Comparator Operation (Continued)

Similarly the operation of IC2b can be summarised as:

Pin 5 < +12V  Pin 8 low.

Pin 5 > +12V  Pin 8 high.

Consider the potential divider R22, the ramp appears at the junction of the two 10K resistors. The ratio of the 10K and 19.25K resistors can be considered as approximately 1:2.




Refer to the above waveforms, whilst the ramp is rising the outputs of IC2 are both low.

When the ramp reaches +18 volts IC2b/5 is at +12V and IC2b/8 goes high switching TR7 on. It will be shown later that this causes the ramp to reverse and so fall. When pin 5 falls below +12V IC2b/8 reverts to the low condition.

The ramp continues to fall and when pin 13 (IC2a) falls to +12V IC2a/1 goes high switching TR6 ON. It will be shown later that this causes the ramp to reverse and so rise. When pin 13 rises above +12V IC2a/1 reverts to the low condition.

3.5.2.1 Comparator Operation (Continued)

Thus the comparators generate positive pulses at ramp voltages of +18V and +6V, the collectors of TR7 and TR6 going high for the same period.

3.5.2.2 Bistable and Latch Operation

TR9/TR10 and associated circuitry form a bistable. TR8 and TR11 have overriding control of the bistable when either is switched on. In the Normal Mode edge connector pin 29 is held low and pin 31 is held high, hence TR8 and TR11 are held off and therefore have no effect.

The positive pulse from IC2a/1, coicident with the ramp falling to +6V, causes TR6 to switch ON for the duration of the pulse, thus applying a high pulse to the base of TR10. TR10 switches on and TR9 is therefore off.

The collector of TR9 goes high causing IC4/4 to go low and IC4/1 to go high.

The positive pulse from IC2b/8, coincident with the ramp rising to +18V, causes TR7 to switch ON for the duration of the pulse, thus applying a high pulse to the base of TR9 causing it to switch on, and TR10 is therefore off.

The collector of TR10 goes high causing IC4/1 to go low and IC4/4 to go high.

Thus when the ramp is rising the positive 30uS RESET pulse is generated at IC4/1 whilst IC4/4 holds TR3 switched off, and TR2 on.

When the ramp is falling RESET is low whilst IC4/4 is high holding TR3 on and TR2 off.

3.5.2.3 Ramp Generation

IC1 is an operational amplifier with TR1 and C6 in the feedback loop. Thus the input on pin 4 is integrated and appears at TR1 emitter.

3.5.2.3 Ramp Generation (Continued)

Under static conditions pin 4 is held at the same voltage as pin 5, with current flowing from 1/10 into TR1 base, holding the emitter of TR1 at +12V.

If pin 4 tries to rise above +12V current flows into pin 4. Since this is the inverting input the current out of 1/10 is reduced by an amount proportional to the closed loop gain of the amplifier.

Thus the current through TR1 is reduced, the emitter voltage falling. The fall is fed back via C6 to 1 pin 4 offsetting the initial rise.

The mechanism operates in reverse for an initial reduction of voltage on 1 pin 4.

When the ramp falls to +6V TR2 is switched on as previously described. TR1 emitter is at +6V and 1 pin 4 is at +12V. Hence C6 is charged to -6V with respect to 1 pin 4.

With TR2 switched on, 1 pin 4 tries to fall towards OV, causing an increase of current to the base of TR1. TR1 conducts more heavily, its emitter voltage therefore rising.

The main current path for C6 is from the +24V rail, via R3, TR1, C6, R20 and TR2 to the OV rail. The rate at which current flows is mainly controlled by the values of R3 and R20 which are selected so that the ramp rises from +6V to +18V in 30uS.

When the ramp reaches +18V TR2 is switched off as previously described. C6 is charged to +6V with respect to 1 pin 4. 1 pin 4 tries to rise towards +24V and the operation detailed above is reversed, i.e. a negative going ramp being generated.

The main current path for C6 is from the OV rail via R4, C6 and:

(a) R9 and R1.

(b) R15 and the Coarse Speed Control.

(c) R16 the Fine Speed Control and R33 to the +24V rail.

3.5.2.3 Ramp Generation (Continued)

The rate at which the current flows is mainly controlled by the values of the Coarse and Fine Speed controls. Hence the slope of the ramp depends on the setting of those controls.

3.5.3 Ramp Generator - Pulsed Mode

In this mode, the ramp generator is normally quiescent. When a single character only is to be transmitted the ramp generator is freed and generates repetitive ramp waveforms as previously described, until completion of the transmission. It then reverts to the quiescent state.

The Pulsed Mode is controlled by signals appearing at edge connector pins 31 and 29. These signals control TR8 and TR11 affording the facility for controlling the bistable TR9/TR10 and hence switching the latch, irrespective of the signals appearing at the comparator output.

In the quiescent period edge connector pins 31 and 29 are held low.

Pin 31 being low makes both TR8 and TR5 conduct.

TR5 conducting makes TR4 conduct applying a short circuit across C6. Thus the output of IC1 is held at +12V, i.e. the same voltage as on IC1 pin 5.

3.5.3 Ramp Generator - Pulsed Mode (Continued)

TR8 conducting:

(a) holds TR10 off.

(b) makes 4/4 high. TR3 conducts holding TR2 off.

Pin 29 being low holds TR11 off.

When the ramp cycle is required:

(a) Pin 31 is taken high for the required duration.

(b) Pin 29 is taken high for 5µS.

Note: The leading edge of both waveforms are coincident.

Pin 31 going high

(a) Switches off TR8 which thus has no further effect on bistable TR9/TR10.

(b) Switches off TR4.

Pin 29 going high switches TR11 on:

(a) Hence TR9 switches off and TR10 on.

(b) The Latch is reset with 4/1 high.

Thus 4/4 goes low switching TR2 on and C6 starts to charge. The voltage across R4 increases from 12V towards 18V.

5µS later, i.e. prior to R4 reaching 18V, pin 29 goes low, TR11 switches off and has no further effect.

3.5.3. Ramp Generator - Pulsed Mode (Continued)

Thus C6 continues to charge and discharge as described in 3.5.2. until pin 31 is taken low. The ramp generator then returns to the quiescent condition.

3.5.4. Comparator Levels

The accuracy of the comparator levels has a direct effect on the accuracy of the speed. To keep these within a close tolerance, R22, a precision potential divider is used to obtain the +6V and +18V switching levels.

The resistors forming the divider are mounted within one package thus providing maximum temperature stability.

R2 provides adjustment to allow for tolerances in:

(a) C6

(b) The divider

(c) The offsets in IC2a and b.

3.5.5. Distortion Generator

The function of the Distortion Generator is to generate a pulse, Sd, of variable duration during the period of each ramp. The pulse is zero whilst the ramp is more positive than the level selected by the DISTORTION control and positive whilst the ramp is more negative. This is described in detail in 2.3.2.

Referring to Figure 8.9., the circuit consists of a comparator IC5 with associated circuitry which may be simplified as shown in Figure 3.2.

3.5.5. Distortion Generator (Continued)

The Ramp voltage is applied to one end of the potential divider R50/R51. The other end is held at a voltage selected by the DISTORTION control, (R2 in Figure 8.6.).

When the voltage on IC5 pin 4 exceeds +12V the output of the comparator, 5/9, is low. When the voltage on pin 4 falls below +12V 5/9 is high.

With 5/9 high TR13 conducts switching on TR14, and 4/13, Sd, goes high.

With 5/9 low TR13 is switched off holding TR14 off. Hence 4/13, Sd is low.

Thus the duration of Sd can be varied over the whole range of the ramp by adjustment of the DISTORTION potentiometer.

With the DISTORTION switch (S15 Figure 8.6.) set to SHORT START or MARK BIAS, the DISTORTION potentiometer is connected to +24V and OV by R21 and R34 respectively. These potentiometers allow for calibration.

At all other positions of the DISTORTION switch, R13 and R46 are used and provide reversal of phase.

3.5.6. Bauds Monitor

4/1 generates positive 30µS RESET pulses coincident with the charging of C6.

The pulses are buffered by emitter follower TR15, and capacitor coupled by C13 to edge connector pin 37. This is connected to the FREQUENCY MONITOR socket on the front panel (Sk. H, Figure 8.6).

3.5.6. Bauds Monitor (Continued)

Protection against excessive external voltages being applied to SK. H is provided by D12, D11 in conjunction with R52 and R54.

3.5.7. + 12V Generation

It is important that the +12V rail is precisely half the voltage of the + 24V rail. Thus two 10K resistors in the R22 package are used as a precision potential divider to provide the input to IC3 pin 5.

The feedback network associated with IC3 ensures that the voltage at the emitter of TR12 is held at precisely half the voltage of the +24V rail.

D8, in conjunction with R38, provides the +6V required by IC5 and IC2.

## 3.6 INTERFACE (Figures 7.4 and 8.10)

### 3.6.1 General

Figure 8.10 shows the circuit diagram and Figure 8.11 shows the more important waveforms. In 3.6.2 to 3.6.11 the Free running mode of operation is assumed. Pulsed operation is then covered in the succeeding sections.

It must be remembered that the Ramp Generator is controlled only by the Serialiser, i.e. when no pulses are available at To or Rp it is because the Ramp Generator is switched off by the Serialiser.

### 3.6.2 ET/LT Generation

The 30uS RESET pulses generated by the Ramp Generator, at twice element frequency, at pin 1, are used to clock the JK Bistable IC2.

In the Free running mode a series of RESET pulses are generated as shown in Figure 8.11(a) and the start element of a five element character is assumed to be as shown. A 1.5 stop element is also assumed.

Since the J & K inputs are held high the Q and $\overline{Q}$ outputs change state at each negative edge of the RESET signals.

Thus the outputs are basically unity mark/space ratio pulses at element frequency. The $\overline{Q}$ and Q outputs are ET (Early Transition) and LT (Late Transition) respectively.

S15h on Figure 8.6 allows selection of either ET or LT to be applied to edge connector pin 28, ET/LT.

The waveforms assume that LT is selected.

With 1:1 reversals not selected pin 35 is high and hence 9/11 is controlled by SLAVE from the Serialiser.

3.6.2 ET/LT Generation (Continued)

SLAVE is normally low and goes high as listed below:

(a) With 1 STOP ELEMENT operation coinciding with the second RESET pulse in the STOP ELEMENT.

(b) With 1.5 STOP ELEMENT operation - coinciding with the third RESET pulse in the STOP ELEMENT.

(c) With 2 STOP ELEMENT operation - coinciding with the fourth RESET pulse in the STOP ELEMENT.

With SLAVE low, 9/11 is high and 8/8 low. Thus 10/6 is high and hence the CLEAR input, 2/2 is held inoperative. Also C8 is held charged via 8/6 which is high.

SLAVE goes high, 9/11 goes low and 8/8 high. Both inputs to 10/6 are high and hence 10/6 goes low clearing IC2 with 2/8 low.

C8 discharges towards OV and in approximately 1uS the low CLEAR pulse at 10/6 is removed. On the succeeding RESET pulse 2/8 goes low coincident with To.

Inverter gates IC8/4 and ICI/13 buffer outputs IC2/8 and IC2/6.

Operation with ET selected is similar.

It should be noted that the CLEAR pulse from 10/6 is only required on switching on the during 1.5 STOP ELEMENT operation.

When 1:1 reversals are selected no CLEAR pulse is applied to the JK bistable.

3.6.3 $\overline{\text{To}}$ and $\overline{\text{Ts}}$ Selection

It can be seen from Figure 8.6 that ET/LT to edge connector pin 28 on the Interface is selected by the DISTORTION switch, S15h.

Signals $\overline{\text{To}}$ and $\overline{\text{Ts}}$ (derived from edge connector pins 27 and 40) are similarly selected by S15g and S15f respectively.

3.6.3 $\overline{To}$ and $\overline{Ts}$ Selection (Continued)

The following table gives details of the settings.

| DISTORTION Switch | Input to pin 28 | $\overline{To}$ derived from pin | $\overline{Ts}$ derived from pin |
|---|---|---|---|
| MARK BIAS | ET | 40 | 37 |
| SPACE BIAS | LT | 37 | 40 |
| OFF | LT | 37 | 40 |
| LONG START | LT | 37 | 40 |
| SHORT START | ET | 40 | 37 |

3.6.4. $\overline{\text{To/Ts}}$ Generation - Pin 37

Refer to Figure 8.10.

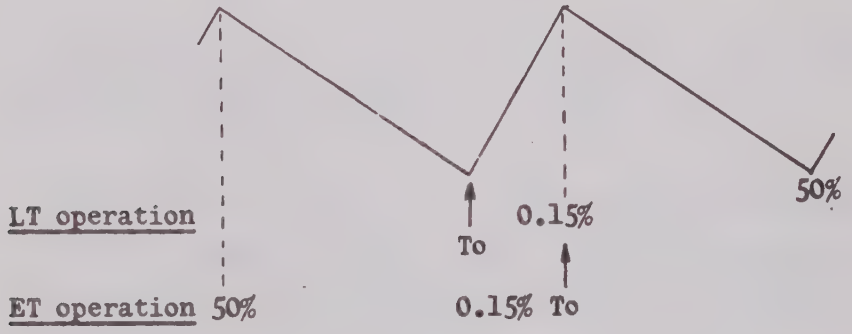
ET/LT and RESET are gated by 9/8, hence alternate RESET pulses are fed out via 12/11 and 12/8 as $\overline{\text{To/Ts}}$ signals.

3.6.5 $\overline{\text{Ts/To}}$ Generation - Pin 40

ET/LT is inverted by 7/13 and then gated with RESET by 11/6. As previously described, 3.6.2., a negative pulse is generated at 10/3 of approximately 5μS duration. This is $\overline{\text{Ts/To}}$.

From 3.5.5. it can be seen that distortion cannot be applied during the flyback period. This is theoretically equivalent to 0.15% at a SPEED of 50 Bauds.

Refer to the following diagram.




With LT operation To coincides with the start of flyback whilst with ET operation To coincides with the end of flyback. Thus at 50 Bauds, the minimum distortion which can be applied is 0.15%, other than with the DISTORTION switch set to OFF.

3.6.6. To and Ts Generation

$\overline{\text{To}}$ from S15g and $\overline{\text{Ts}}$ from S15f respectively, Figure 8.6., are inverted by 6/6 and 3/13 respectively to become To and Ts.

3.6.7. Td Generation

Sd on edge connector pin 38 is generated on the Ramp Generator. It is a series of positive pulses, the duration of each pulse being as set by the DISTORTION potentiometer.

Sd is gated by the inverted ET/LT signal at 11/8 as shown in the waveforms, Figure 8.11(a).

11/11 ensures that Td always goes negative coincident with 11/6 going positive.

Hence Td is a train of positive pulses, the duration of each pulse being set by the DISTORTION potentiometer.

With LT selected Td occurs between To and Ts, whilst with ET selected Td occurs between Ts and To.

If the DISTORTION potentiometer is not correctly calibrated the following abnormal conditions can occur:

(a) With the potentiometer set to 50% Sd may be permanently low. Td must go high at 50%. This is achieved by the output of 11/6 going high at the start of $\overline{Ts/To}$.

(b) With the potentiometer set to 0% Sd may be permanently high. Td must go low at 0%. This is achieved by the output of 1/4 going low at the start of $\overline{To/Ts}$.

3.6.8. CODER Generation

$\overline{CODER}$ is generated once per character by the Serialiser. It is gated with $\overline{To}$ at 7/10 becoming CODER, a negative pulse used at the Message Generator.

3.6.9. Oscillator Run Operation

In 3.6.3. a positive 5μS pulse coincident with the start of OSC RUN was required. This pulse is generated on the Interface.

OSC RUN is normally low, holding 11/3 low, via 10/11. Also 8/12 is high and C6 is charged.

OSC RUN going high makes 10/13 high and 8/12 low. C6 holds 10/12 high for 5μS and hence 10/11 goes low for 5μS, reverting to high when C6 has discharged sufficiently.

3.6.10 $\overline{\text{RUN}}$ Generation

4/11 and 4/8 form a bistable which is set by edge connector pin 26 going low and reset by pin 36 going low. The purpose of the bistable is to obviate contact bounce on the RUN/STOP switch, S11 in Figure 8.6.

With the RUN/STOP switch at STOP 4/8 is high, hence $\overline{\text{RUN}}$ is high.

With the switch at START 4/8 is low and hence $\overline{\text{RUN}}$ is low.

3.6.11. Free Running Operation

Figure 8.11 (b) shows the waveforms when the equipment is in the free running mode and for a Test message being transmitted.

The important outputs are:

(a) Pin 19 - this is connected to the serialiser Pin 20 and is held low whilst the STOP/RUN switch is at RUN.

3.6.11. Free Running Operation (Continued)

(b) Pin 21 - this provides a continuous train of To pulses whilst at RUN. At STOP the Ramp Generator is switched off. Note that although pulses may appear at 12/6 they are inhibited.

(c) Pin 7 - this is connected to the Serialiser pin 29 and consists of alternating $\overline{To}$ and $\overline{Ts}$ signals except when 1.5 STOP ELEMENT is selected. In that case only $\overline{To}$ pulses are provided.

When the RUN/STOP switch is set to STOP, $\overline{SM}$ is not generated until the end of the final character of the message being transmitted.

Figure 8.11(c) is similar to the description above and shows operation when a character is selected on KEYS.

The basic difference is that when the RUN/STOP switch is set to STOP, $\overline{SM}$ is generated at the end of the character being transmitted.

3.6.12. Pulsed Operation

3.6.12.1. General

In the Pulsed mode, triggering pulses are derived either from

(a) the STEP button

or (b) an external source.

On the relevant waveforms the triggering pulses are assumed to be from an external source.

### 3.6.12.2. STEP Button Operation

Operating of the STEP button causes edge connector pin 33 to go low. When the button is not operated pin 34 is low.

9/3 and 9/6 form a bistable preventing push button bounce being transmitted into the logic.

TR1 and TR3 form a monostable whose duration is governed by C5 and R17. The period is 15μS approximately.

When the push button is operated, 9/3 goes high switching TR2 on. TR2 conducting holds the base of TR3 low.

TR3 is thus switched off holding TR1 on. Thus, if the push button is released TR1 will remain conducting until C5 discharges, i.e. for 15μS from operating the button.

After 15μS C5 allows TR3 to conduct switching TR1 off.

Hence the input to 12/2 is a positive 15μS pulse whose leading edge is coincident with the pressing of the STEP button.

### 3.6.12.3. External Trigger Pulse

If a positive edge trigger pulse is used, LKB only is connected, LKA and LKC being left open.

If a negative edge trigger pulse is used, LKA and LKC are connected, LKB is left open. In this case TR4 is used to invert the trigger pulse.

Thus, with a trigger pulse applied TR1 base is always taken positive, switching TR1 on.

The action of monostable TR1/TR3 is described in 3.6.12.2.

### 3.6.12.4. Pulsed Mode Operation

Figure 8.11.(d) shows the waveforms when the equipment is in the Pulsed mode and a Test Message is being transmitted.

The important outputs are:

(a) Pin 19 - this is connected to the Serialiser pin 20, and is held high during pulsed operation.

(b) Pin 21 - this provides blocks of pulses, each block initiated by the trigger pulse. The number of pulses depends on whether the 5 or 8 element code is used.

(c) Pin 7 - this is connected to the Serialiser Pin 29 and consists of blocks of alternating $\overline{To}$ and $\overline{Ts}$ signals except when 1.5 ELEMENT STOP is selected. In that case only $\overline{Ts}$ signals are provided. This is shown in Figure 8.11.(f).

When the RUN/STOP switch is set to STOP, $\overline{SM}$ is not generated until the end of the final character of the message being transmitted. This is clearly shown in Figure 8.11.(d), the switch having been flicked to RUN and then to STOP.

Figure 8.11.(e) is similar to the description above and shows pulsed operation when a character is selected by KEYS.

The basic difference is that when the RUN/STOP switch is set to STOP, $\overline{SM}$ is generated at the end of the character being transmitted.

## 3.7. MESSAGE GENERATOR (Figures 7.5 and 8.12)

### 3.7.1. General

The output of this board is parallel data obtained from either the KEYS or the R.O.M. Either 5 or 8 element codes can be selected.

The R.O.M. is addressed by means of a counter and contains:

(a) Short Test Message

(b) Medium Test Message

(c) Long Test Message

Details of the Test Messages are given in Figure 8.4.

The circuit diagram is shown in Figure 8.12.

### 3.7.2. Read Only Memory

#### 3.7.2.1. General

Figures 3.3.(a) and (b) show details of the R.O.M.

The logic levels for the R.O.M. are:

Low level + 24V

High level 0V

TR1 to TR7 inclusive perform the transition of R.O.M. logic levels to TTL levels. Similarly ICs 2 and 3 are used to perform the transition of TTL levels to R.O.M. levels in conjunction with pull up resistors R17 to R23 and R12 to R16.

3.7.2.1. General (Continued)

Consider the first five columns in Figure 3.3.(a). Columns $C_A$, $C_B$ and $C_C$ are associated with the Long Test Message, Column $C_D$ is associated with the Medium Test Message, and Column $C_E$ is associated with the Short Test Message. This is shown by the top left hand block in Figure 3.3.(b).

This block is addressed by $I_1$ to $I_6$ inclusive, being low.

Each column is addressed by the appropriate C line going low, when the contents of the column appear at outputs O1 to O7 inclusive.

3.7.2.2. 5 or 8 Unit Code Selection

With reference to Figure 3.3.(a) it can be seen that the first and third rows contain 8 level data, whilst the second and fourth rows contain 5 level data.

Selection of the first and third rows is achieved by making $I_6$ low.

Refer to Figure 8.12. With 8 level data $\overline{8L}$ is low, 2/6 is high and hence I6 is held at + 24V via R17.

Similarly selection of the second and fourth rows is achieved by making $I_6$ high, i.e. OV. With 5 level data selected $\overline{8L}$ is high, 2/6 is low and hence $I_6$ is held at OV.

3.7.2.3. Long Test Message Selection

Assume 8 level code has been selected.

With the Long Test Message selected only $C_A$ is enabled initially, $C_B$ to $C_E$ being inhibited. How this is achieved will be shown later.

3.7.2.3. Long Test Message Selection (Continued)

$I_1$ to $I_6$ are all low and thus the contents of $C_A$ in the first block are applied to the outputs 01 to 07 inclusive. This constitutes the parallel data for the first character of the Long Test Message.

When transmission of this character is completed $I_4$ only is taken high, thus addressing column $C_A$ in the second block of the first row. The data for the second character of the Long Test Message is now available at the outputs.

This sequence is repeated until all sixteen blocks in the first row have been addressed sequentially.

$I_5$ then goes high and the first block in the third row, i.e. still 8 level code, is addressed.

The blocks in the third row are addressed sequentially and at the end 32 characters will have been transmitted.

The two rows are again addressed sequentially with column $C_B$ only enabled, followed by the two rows with column $C_C$ only enabled.

In this manner the parallel data for each of the 96 characters constituting the Long Test Message is sequentially available at the outputs.

3.7.2.4. Medium Test Message Selection

The Medium Test Message is obtained from column $C_D$ in the relevant two rows. Addressing is achieved in a similar manner as described in 3.7.2.3.

3.7.2.4. Medium Test Message Selection (Continued)

The two rows are only addressed once per Medium Test Message thus generating the 32 characters required.

3.7.2.5. Short Test Message Selection

The Short Test Message of 8 characters is contained in the first eight blocks of rows one and two. Only column $C_E$ is addressed in a similar manner as described in 3.8.2.3.

3.7.3 Test Message Generation

3.7.3.1. Long Test Message

IC7, 6 and 5/5 form a five bit binary counter. IC5/9 and IC4 form a three bit shift register.

SLAVE pulses high during the stop element of a character, i.e. once per character, and is used to clock the counter.

The Q outputs of the counter are used to control the R.O.M., $I_1$ to $I_5$ inclusive. $I_6$ is controlled by $\overline{8L}$ as described in 3.8.2.3. $I_7$ is held permanently low, i.e. at +24 via R23 and 3/2, and is thus inoperative.

IC 14/6 and 12/8 form a bistable, 12/8 going low clears the counter and the shift register with all Q outputs low.

Assume the following:

(a) 12/8 is low, hence 14/6 is high.

(b) the RUN/STOP switch is at STOP and hence $\overline{\text{RUN}}$ is high.

(c) the CHARACTER switch is at LONG TEST MESSAGE, hence $\overline{\text{MED MESSAGE}}$, $\overline{\text{SHORT MESSAGE}}$, and $\overline{\text{KEYS}}$ are high.

(d) $\overline{\text{SM}}$ is low.

3.7.3.1. Long Test Message (Continued)

With $\overline{\text{KEYS}}$ high 13/8 is low thus 11/4 is controlled by $\overline{\text{RUN}}$. When $\overline{\text{RUN}}$ is high 11/4 is low inhibiting Cp at 12/11. When $\overline{\text{RUN}}$ is low 11/4 is high and the Cp pulses pass through 12/11. CP is generated by the To occurring in the start element of a character.

Thus when the RUN/STOP switch is set to RUN:

(a) 12/6 goes low terminating $\overline{\text{SM}}$.

(b) 11/4 goes high enabling 12/11.

Cp pulsing high makes 12/11 pulse low, 12/8 goes high freeing the counter and shift register.

The counter is clocked by SLAVE selecting $I_1$ to $I_5$ on the R.O.M. as required by 3.8.2.3.

Consider the inputs into 14/8:

(a) Pin 9 is held high by $\overline{\text{KEYS}}$.

(b) Pin 10 is held high by $\overline{\text{SINGLE MESSAGE}}$.

(c) Pin 12 is held high by 11/13, since 5/9 and 4/8 are both low.

(d) Pin 13 is held high by $\overline{\text{MED MESSAGE}}$.

Thus 14/8 is low and R.O.M. column $C_A$ is selected. It can be seen that the remaining columns, $C_B$ to $C_E$ are inhibited.

At the completion of the first count of 32, the high on 11/13 is clocked by 5/6 into 5/9 which goes high.

3.7.3.1 Long Test Message (Continued)

11/13 goes low making 14 pin 12 low and hence 14/8 goes high inhibiting column $C_A$.

5/9 going high selects column $C_B$ via 2/2. The counter continues counting again selecting $I_1$ to $I_5$ on the R.O.M. as required by 3.8.2.3.

At the completion of the second count of 32, i.e. on count 65, 4/8 goes high. The low on 11/13 is clocked into 5/9 which goes low.

5/9 going low makes 2/2 high inhibiting column $C_B$.

4/8 going high:

(a) holds 11/13 low and hence via 14/8 holds column $C_A$ inhibited.

(b) enables column $C_C$ via 2/12.

The counter continues counting until the third count, i.e. count 96, is completed.

At the start of count 96 all Q outputs of the counter are high. 4/6 is low and hence 10/3 is high.

Thus all the inputs to 8/8 are high with the exception of CODER. With reference to Figure 8.11.(a) it can be seen that CODER goes high at the beginning of the STOP element. However, by this time the character data from the R.O.M. has already been processed by the Serialiser and CODER going high makes 8/8 low.

3.7.3.1. Long Test Message (Continued)

8/8 going low makes 14/6 high and 12/8 goes low clearing the counter and shift register as previously described. Thus another cycle can be initiated.

The RUN/STOP switch may be set to STOP at any time during the cycle of events when $\overline{\text{RUN}}$ will go high enabling 12/6.

The cycle continues until the next count 96 is reached. 14/6 goes high as described above, and hence 12/6 goes low, clamping the Counter at Reset and starting $\overline{\text{SM}}$ as shown in Figure 8.11.(b),(c),(d) and (e).

Thus transmission of a Long Test Message only stops at the end of the message.

3.7.3.2. Medium Test Message

Operation with Medium Test Message selected is similar to that described in 3.8.3.1.

The only difference in the input signals is that $\overline{\text{MED MESSAGE}}$ is held low.

Thus:

(a) 10/3 is held high.

(b) 14/8 is held high inhibiting column $C_A$.

(c) 2/10 is held low selecting column $C_D$, i.e. the Medium Message column.

Since 10/3 is held high 8/8 goes low, at CODER, during the count of 32. Thus the cycle consists of 32 characters.

3.7.3.2. Medium Test Message (Continued)

When the RUN/STOP switch is set to STOP the cycle continues until CODER is generated during the thirty second count. $\overline{SM}$ then goes low and the cycles are stopped.

3.7.3.3. Short Test Message

Operation with Short Test Message selected is similar to that described in 3.8.3.1.

The only difference in the input signals is that $\overline{\text{SHORT MESSAGE}}$ is low.

Thus:

(a) 14/8 is held high inhibiting column $C_A$.

(b) 2/8 is held low selecting column $C_E$, i.e. the Short Message column.

(c) 12/3 is enabled. Note - with Long and Medium Test Messages 12/3 is held permanently high.

Since 12/3 is enabled, it goes low on a count of eight. 14/6 thus goes high, making 12/8 low and thus clearing the counter. Thus only eight characters are generated per cycle.

$\overline{SM}$ is again only generated at the end of the Short Test Message being transmitted when the RUN/STOP switch is set to STOP.

3.7.4. Single Character Operation

With the CHARACTERS switch set to KEYS:

(a) $\overline{\text{KEYS}}$ is held low, holding 14/6 permanently high.

(b) $\overline{\text{SHORT MESSAGE}}$ and $\overline{\text{MED MESSAGE}}$ are held high.

3.7.4. Single Character Operation (Continued)

Assume the RUN/STOP switch is at STOP then $\overline{RUN}$ is high and thus $\overline{SM}$ is low.

When the RUN/STOP switch is set to RUN, $\overline{RUN}$ goes low. $\overline{SM}$ goes high. 11/4 goes low inhibiting the Cp pulses. Hence 12/8 is held low and the counter and shift register are held in the cleared condition.

$\overline{KEYS}$ being low also inhibits selection of column $C_A$ at 14/8. $C_B$ to $C_E$ are also inhibited, hence all the outputs of the R.O.M. 01 to 07 are high enabling the output gates for the KEY data.

The outputs from the Message Generator board are thus as selected by the setting of the KEYS, S2 to S8 inclusive, Figure 8.6.

It must be noted that when the CHARACTER switch is not at KEYS all the input lines are held high by the +5V rail via R35 to R41 inclusive, hence enabling the output gates for the R.O.M. data.

3.7.5 Continuous Operation

For continuous operation $\overline{RUN}$ is held low and $\overline{KEYS}$ is high. Thus both inputs to 11/4 are low and 11/4 is held high.

When Cp goes high 12/11 goes low resetting the bistable formed by 14/6 and 12/8 with 12/8 high. The counter is therefore freed and a fresh sequence of operation is initiated.

3.7.6 Serial Logic and Dry Contact Outputs

The logic circuit comprising IC1, TR8 and associated components provides the following outputs of the serial data fed from the Serialiser PCB via pin 4:

(a) Logic level output at pin 10 which is fed via the electronic output PCB to the equipment under test.

3.7.6 Serial Logic and Dry Contact Outputs (Continued)

(b) Logic level at pin 5 and dry contact signal at pin 3. The logic signal is fed to a socket on the front panel and both signals are fed to terminal block TB2. This enables the serial data to be applied to additional equipment in either of these forms if required. Links are provided to enable an OV dry contact signal to be obtained when either positive or negative mark is selected by means of MARK polarity key (+ve mark - link B to C, -ve mark - link A to B).

## 3.8 SERIALISER

### 3.8.1 General

The functions of the Serialiser are as follows:

(a) to convert parallel character data from the Message Generator into the serial form required by the Electronic Output.

(b) to generate the one bit START element.

(c) to generate a STOP element of the required duration.

(d) to insert the appropriate PARITY bit when required.

(e) to introduce DISTORTION as required.

(f) to provide 1:1 reversals.

(g) to provide continuous MARK or continuous SPACE outputs when required.

The operation of the Serialiser can be conveniently broken down into the five blocks shown in Figure 2.1. The blocks are labelled in the circuit diagram shown in Figure 8.13.

Figures 8.14, 8.15 and 8.16 show relevant waveforms associated with Serialiser operation.

### 3.8.2 Counter and Multiplexer Operation

#### 3.8.2.1 8 Level Count

Refer to Figure 8.14.

3.8.2.1 8 Level Count (Continued)

The following settings are assumed to be made:

(a) SIGNAL switch set to CHARACTERS; CH. SW., edge connector pin 36, held low.

(b) STOP ELEMENT switch set to 8 level CODE, 2 bit STOP ELEMENT; $\overline{8L}$ and $\overline{2}$ held low, $\overline{5L}$ held high.

(c) RUN/STOP switch at STOP.

Thus the initial waveforms are as shown, neglecting the Counter and Multiplexer states.

When the RUN/STOP switch is set to RUN, edge connector pin 20 goes low taking OSC RUN high and the Ramp Generator runs.

The first To pulse generated appears at pin 18, To or $R_P$, and 10/6 goes low. This is a reset pulse for the counter bistables. 8/9 is reset low, whilst 8/5, 5/8, 17/5 and 17/9 are reset high.

Hence 10/6 goes high whilst SLAVE goes low.

8/9 and 5/8 are clocked by Ts, and 17/9 is clocked by alternating $\overline{To}$ and $\overline{Ts}$ from the Interface.

The waveforms show that the output of the Multiplexer (i.e. 11/11) consists of data from the Message Generator, U1 - U7, followed by the parity bit P, with an interval of three bits, allowing for a 1-bit START element and a 2-bit STOP element.

3.8.2.2 5 Level Count

Refer to Figure 8.15.

The following settings are assumed to be made:

(a) SIGNAL switch set to CHARACTERS; CH. SW., edge connector pin 36, held low.

(b) STOP ELEMENT switch set to 5 level CODE, 1.5 STOP ELEMENT; $\overline{8L}$ and $\overline{2}$ held high, $\overline{5L}$ held low.

(c) RUN/STOP switch at STOP.

Thus the initial waveforms are as shown, neglecting the Counter and Multiplexer states.

When the RUN/STOP switch is set to RUN the action is similar to that detailed in 3.7.2.1.

8/9 and 5/8 are clocked by Ts, whilst 17/9 is clocked by $\overline{To}$ only from the Interface, since 1.5 STOP ELEMENT is selected, see Figure 8.11.

It can be seen that the output of the Multiplexer at 11/11 is the parallel data from the Message Generator, U1 - U5, with an interval of two and a half bits allowing for 1 bit START element and 1.5 STOP element.

3.8.2.3 Termination of Counter Operation

Basically two conditions are required for termination of counter operation:

(a) Edge connector pin 20 must be high.

(b) SLAVE must be high.

3.8.2.3 Termination of Counter Operation (Continued)

It can be seen from Figures 8.14 and 8.15 that SLAVE only goes high at the end of each complete count. Thus, in all circumstances, a character in the process of being transmitted is completely transmitted before the counter operation is terminated.

Remembering that the counter only operates whilst the SIGNAL switch is at CHARACTERS, pin 20 going high can be initiated in several ways as listed below:

(a) With the CHARACTER switch at TEST MESSAGE, the RUN/STOP switch is set to STOP.

At the Interface, Figure 8.11, $\overline{SM}$ does not go low until the end of the Test Message being transmitted. Thus pin 20 is held low until the last character of the Message is being transmitted.

Pin 20 goes high during the transmission of the last character and counter operation is terminated by SLAVE going high at the end of the last character.

(b) With the CHARACTER switch at KEYS, the RUN/STOP switch is set to STOP.

Pin 20 immediately goes high, see Figure 8.11, and counter operation is terminated by SLAVE going high at the end of the character being transmitted.

(c) The OUTPUT switch is set from CHARACTERS to any other position. Pin 20 immediately goes high and counter operation is terminated by SLAVE going high at the end of the character being transmitted.

3.8.2.3 Termination of Counter Operation (Continued)

It must be noted that SLAVE being low inhibits the operation of continuous MARK, continuous SPACE and 1:1 reversals via 19/8 which is held high.

3.8.2.4 Selection of Code

From Figure 8.6. it can be seen that with:

(a) 8 level CODE selected; $\overline{8L}$ is low and $\overline{5L}$ is high.

(b) 5 level CODE selected; $\overline{8L}$ is high and $\overline{5L}$ is low.

From the previous two subsections it can be seen how the counter operation is controlled by these signals.

3.8.2.5 Selection of STOP ELEMENT Duration

2 STOP ELEMENT operation holds $\overline{2}$ low, and the counter operation is shown in Figure 8.14.

1.5 STOP ELEMENT selected holds $\overline{1.5 \text{ EL. STOP}}$ low on the Interface. This has the effect of switching the ET/LT bistable on the Interface and so causing the last To of a character to be followed by the first To of the next character without an intervening Ts. This is clearly shown in Figure 8.11. The action on the counter is shown in Figure 8.15.

3.8.2.5 Selection of STOP ELEMENT Duration (Continued)

1 STOP ELEMENT operation is achieved by $\overline{2}$ and $\overline{1.5 \text{ EL STOP}}$ both being high. Thus the action of the counter is modified so that the output of the Multiplexer is parallel data with two bit intervals, allowing for 1 STOP element and 1 START element.

3.8.2.6 Trigger and Cp Generation

With CHARACTERS not selected CH.SW. is held high hence 19/3 is held low, holding 19/6 high. Thus Cp is held high.

With Cp high, TR2 conducts, holding TR1 on. TR1 collector is held at +5V approximately. C2 is charged and therefore TRIG OUT is OV.

With CHARACTERS selected CH.SW. is held low, 19/6 is normally low and pulses high coincident with 10/6 pulsing low.

Thus Cp is normally low, pulsing high when 10/6 pulses low.

TR2 is normally cut off, holding TR1 off. C2 is discharged. When TR2 conducts under the influence of Cp going positive, TR1 conducts taking TRIG OUT high.

D1, D2, R19 and R2 protect the circuit from any externally applied voltage

3.8.3 Parity Generation

The Parity Generator bistable is cleared by 10/6 pulsing low at the start of each character.

The bistable is clocked by Ts.

3.8.3 Parity Generation (Continued)

When the output of 11/11 is low the bistable remains as previously set. When 11/11 is high the bistable changes state.

When EVEN PARITY is selected $\overline{\text{ODD PARITY}}$ is high, holding 15/6 high and thus 15/3 is controlled by 14/8.

When ODD PARITY is selected $\overline{\text{ODD PARITY}}$ is low, holding 15/8 and 15/11 high and thus 15/3 is controlled by 14/6.

For example assume:

(a) 8 level code selected with odd parity.

(b) a character 1001111

then bistable switching will be as follows.

| Time | 11/11 | 14/6 |
|---|---|---|
| To 1 | | 1 |
| Ts 1 | 1 | 0 |
| Ts 2 | 0 | 0 |
| Ts 3 | 0 | 0 |
| Ts 4 | 1 | 1 |
| Ts 5 | 1 | 0 |
| Ts 6 | 1 | 1 |
| Ts 7 | 1 | 0 |
| Ts 8 | 0 | |

Thus the Parity bit, P, is 0 at Ts 8 as required for odd parity.

## 3.8.4 Output Operation

### 3.8.4.1 Introduction

The Output stage consists of IC18, a JK bistable clocked by Ts.

When CHARACTERS is not selected the bistable is controlled by the J and K inputs, the CLEAR and PRESET inputs being held high.

When CHARACTERS is selected the CLEAR and PRESET inputs are used to control the bistable.

18/8 supplies the output for +VE MARK polarity, whilst 18/6 supplies the output for -VE MARK polarity. In the following description only +VE MARK polarity is considered.

### 3.8.4.2 1 : 1 Reversals Generation

When 1 : 1 reversals is selected CH. SW is held high. SLAVE is also high. Thus 19/8 is held low. 17/9 is held clear by the low on 17 pin 13. Refer to Figure 8.16(D).

19/8 being low also holds 7/6 and 16/6 high. Thus the CLEAR and PRESET inputs to IC18 are held inoperative.

IC18 pins 3, 4, 10 and 11 are held high, by the +5V rail via R16 and R14. Pins 5 and 9 are held low by 19/8. Thus the J and K inputs are both high.

Hence the bistable changes state at each Ts clock pulse. Thus the output is 1 : 1 reversals.

3.8.4.3 Continuous MARK Generation

With the SIGNAL switch at MARK, $\overline{\text{MARK}}$ edge connector pin 31, is held low. Thus the K input to IC18 is held low and 18/8 is thus clocked high by the first Ts clock pulse and remains high thereafter.

Should a continuous MARK generation be selected when a character is being transmitted SLAVE is low. Hence 19/8 is high and continuous MARK generation is inhibited at IC18 since the J and K inputs are held low.

When the character is completely transmitted, SLAVE goes high and continuous MARK generation is initiated as described above. At continuous MARK, CH.SW. is high. When SLAVE goes high 19/8 goes low holding 17/8 high. Thus SLAVE remains high. When the SIGNAL switch is moved to CHARACTERS, CH.SW. goes low freeing IC17.

3.8.4.4 Continuous SPACE Generation

With the SIGNAL switch at SPACE, $\overline{\text{SPACE}}$, edge connector pin 26, is held low. Thus the J input to IC18 is held low and 18/8 is clocked low by the first Ts clock pulse and remains low thereafter.

Should continuous SPACE generation be selected when a character is being transmitted SLAVE is low. Hence 19/8 is high and continuous SPACE generation is inhibited at IC18 since the J and K inputs are held low.

3.8.4.4 Continuous SPACE Generation (Continued)

When the character is completely transmitted, SLAVE goes high and continuous SPACE generation is initiated as described above. At continuous SPACE, CH.SW. is high. When SLAVE goes high 19/8 goes low holding 17/8 high. Thus SLAVE remains high.

When the SIGNAL switch is moved to CHARACTERS, CH.SW. goes low freeing IC17.

3.8.4.5 Character Operation

With the SIGNAL switch set to CHARACTERS, and the RUN/STOP at RUN, SLAVE is normally low, hence IC18 J and K inputs are held low. The bistable is then controlled by 7/6 and 16/6 as will be shown in subsection 3.8.5.

3.8.5 Data Controller Operation

3.8.5.1 DISTORTION Switch at OFF

Operation of the Data Controller logic with the DISTORTION switch at OFF is shown in Figure 8.16.(A).

$\overline{\text{DISTORTION}}$ and $\overline{\text{BIAS}}$ are held high, whilst $\overline{\text{DIST. OFF}}$ is held low.

START is derived from signal To or Rp fed via contacts on S15C (see Figure 8.6).

In the waveform the character 1001111 followed by 1101111 has been assumed.

Thus the output at 18/8 is undistorted data as shown.

3.8.5.2 DISTORTION Switch at LONG START

The operation of the Data Controller logic is shown in Figure 8.16(B), with LT selected as described in section 2.4.

$\overline{\text{BIAS}}$ and $\overline{\text{DIST OFF}}$ are held high, and $\overline{\text{DISTORTION}}$ is held low.

It can be seen that all data elements are of the correct duration. Alteration of Td only increases the duration of the START element and correspondingly decreases the duration of the STOP element.

3.8.5.3 DISTORTION Switch at SHORT START

By selection of ET as described in section 3.4. Td is effectively shifted through half an element.

Thus, all data elements will be of the correct duration and alteration of Td only decreases the duration of the START element and correspondingly increases the duration of the STOP element.

3.8.5.4 DISTORTION Switch at MARK BIAS

The operation of the Data Controller logic is shown in Figure 8.16(C) with LT selected as described in Section 2.4.

$\overline{\text{DISTORTION}}$ and $\overline{\text{BIAS}}$ are both held low, and $\overline{\text{DIST OFF}}$ is held high.

It can be seen that the start point of MARK elements depends upon the setting of Td and they can be made to occur earlier than To. The duration of the SPACE elements are correspondingly decreased.

3.8.5.5 DISTORTION Switch at SPACE BIAS

By selecting ET as described in section 2.4. Td is effectively shifted through half an element.

3.8.5.5 DISTORTION Switch at SPACE Bias (Continued)

Thus the end point of MARK elements depends upon the setting of Td and they can be made to occur later than To. The duration of the SPACE elements are correspondingly increased.

3.8.6 Pulsed Operation

Operation of the Serialiser in the pulsed mode is initiated by the Rp pulse generated at 5/8 on the Interface board.

Rp appears at the Serialiser as:

(a) a positive 15μS pulse on edge connector pin 18, To OR Rp.

(b) a negative 15μS pulse on edge connector pin 29.

Edge connector pin 20 is held permanently high.

To OR Rp going high makes 10/6 low thus resetting the relevant counter bistables. Hence 16/12 goes high.

Edge connector pin 29 goes low and then high at the end of Rp clocking 17/9. 17/9 goes high and 17/8 low, i.e. SLAVE low.

17/8 going low:

(a) takes 10/6 high thus freeing the counter.

(b) takes OSC RUN high and the Ramp Generator runs producing the To and Ts signals. Note that the first To is only 15μS duration, i.e. only half a RESET pulse is generated.

3.8.6 Pulsed Operation (Continued)

The counter operates for one count only, i.e. until SLAVE goes high and the counter stops until the next Rp pulse appears.

Thus for each release pulse one character only is transmitted.

## 3.9 ELECTRONIC OUTPUT (Figures 7.7 and 8.17)

### 3.9.1 General

The function of the Electronic Output is to convert the signals into a suitable form for transmission.

The polarity of the signals is controlled by the data from the Serialiser via the MARK POLARITY switch.

The amplitude of the signals is controlled by the +VE and -VE inputs which are derived from the SUPPLY switch.

### 3.9.2 Outline of Operation

Figure 3.4 shows a Block Diagram of the Electronic Output.

Data from the Serialiser is used to switch the output of a 1MHz OSCILLATOR to DRIVER 1 or DRIVER 2.

The outputs of the DRIVERS are transformer coupled to the OUTPUT circuits.

The OUTPUT circuits consist of a rectification and smoothing circuit, D1/L1 and D2/L2.

The d.c. outputs are used to control switching transistors, TR1 and TR2.

Assume that:

(a) The TELEGRAPH BATTERY is selected.

(b) +VE MARK POLARITY is selected.

3.9.2 Outline of Operation (Continued)

(c) The output of the Serialiser is at MARK.

Thus the +VE voltage at the OSCILLATOR switch connects the output of the oscillator to DRIVER 2. Thus DRIVER 2 generates an output which is rectified, applying a positive voltage to TR2 which conducts switching the +VE voltage from the TEL. BATT to LINE.

There being no output from DRIVER 1, TR1 does not conduct and there is an open circuit between -VE voltage and LINE.

When the output from the Serialiser goes to SPACE TR1 conducts applying -VE to LINE, whilst TR2 provides an open circuit between +VE and LINE.

3.9.3 Oscillator Operation

Refer to Figure 8.17.

The 1MHz oscillator is formed by TR14/TR15 and associated circuitry.

On switching on, both transistors may be conducting and hence TR9 and TR10 are both cut off. In this case C1 charges, switching off either TR15 or TR14. Hence the bistable action is started. TR9 and TR10 then conduct alternately holding C1 discharged.

The outputs of the oscillator are taken out via D6 and D7.

3.9.4 Data Switching

Data from the MARK POLARITY switch, S16 on Figure 8.6., is applied to edge connector pin 7.

Assume this input is high, then TR4 is conducting making TR12 conduct, and, via D1, D3 and D2, holding TR13 off.

3.9.4 Data Switching (Continued)

TR12 controls the supply for DRIVER 2 whilst TR13 controls the supply for DRIVER 1.

3.9.5 Driver Operation

DRIVER 2 operation only is described since operation of DRIVER 1 is similar.

Assume TR12 is off then no supply is available for TR3 and TR11, TR1 and TR2 are not conducting.

Assume TR12 is conducting then the supply is available for TR3 and TR11. These two transistors are controlled by the outputs of the 1MHz OSCILLATOR, hence they switch on and off at 1MHz. Thus TR1 and TR2 switch on and off at 1MHz, generating a.c. in the transformer.

3.9.6 Output Circuit

Since the operation of OUTPUT 1 and 2 circuits is similar, only circuit 1 is described.

The a.c. from the transformer T2 is full wave rectified by D9 and D8, smoothing being applied by L2.

The positive voltage applied to the base of TR20 switches it on and it conducts thus connecting LINE to +VE VOLTS IN.

TR16 is also switched on by the positive voltage from the rectifier, and holds TR17 off.

When TR1 and TR2 are switched off, i.e. the input on edge connector pin 7 goes low, TR16 switches off. C6 charges due to the current through L1 and TR17 conducts shunting the current from L2 to TR20 base. Thus TR20 is switched off rapidly.

3.9.7 Protection

TR20 is protected from overload by TR22 and TR21 in association with LINKS A1, A2, A3 and A4. The links are set up so that if the current through TR20 exceeds 250mA, TR22 conducts.

TR22 conducting causes TR21 to conduct which

(a) holds TR22 on

(b) shunts the current to TR20 base and thus switches it off. TR20 remains shunted whilst TR21 conducts.

TR21 only stops conducting when no power is applied to T2.

The action of TR25, TR24 and LINKS B1, B2, B3 and B4 is identical on TR23.

Protection against the batteries being incorrectly connected, or voltages in excess of 200V being applied to LINE is provided by diodes D14 and D15.

## 3.10 OPTIONAL MESSAGE GENERATOR (Figures 7.8 and 8.18)

The Optional Message Generator board can be incorporated in the TSG 40.2 as an optional extra to generate special test messages to customers' requirements.

128 characters are available in both 5-level and 8-level codes so that long, medium and short test messages containing any number of characters up to the following maxima may be programmed for each message.

(i) Long test message - 96 characters

(ii) Medium test message - 24 characters

(iii) Short test message - 8 characters

The test messages are stored in two Read-Only Memories which are plugged into sockets.

If the test messages are to be changed after initial manufacture suitably programmed Read-Only Memories can be plugged in to replace the existing units.

The Read-Only Memories are readily available in both field and mask programmable orientations.

### 3.10.1 Circuit Description

#### 3.10.1.1 Character Storage

The circuit diagram and board layout are shown in Figures 8.19 and 7.8 respectively.

Character storage is provided in two Read-Only Memories, IC3 and IC8, each containing 1024 bits arranged as 256 words of 4 bits.

The Read-Only Memories (ROM's) are connected to provide 256 8-bit words, each programmed word being one character.

3.10.1 Character Storage (Continued)

128 of the 256 characters are arranged in each operate code.

A ROM is enabled when CE is taken low, is addressed at inputs $A_0$ to $A_7$ inclusive and has outputs at $O_1$ to $O_4$. Outputs are at normal logic levels.

3.10.1.2 Code Selection

When $\overline{8L}$ on pin 6 is taken low the first 128 addresses of the ROMs are selected via inputs $A_7$ permitting the generation of 8-level messages. When $\overline{8L}$ is taken high the second 128 addresses are selected permitting the generation of 5-level test messages.

3.10.1.3 Storage Addressing

IC2 and IC4 form an 8-stage character counter, seven stages of which address ROM inputs $A_0$ to $A_6$ sequentially to generate the relevant test message. The eighth stage of the counter is unused.

The length of message generated is determined by inputs $\overline{\text{SHORT MESSAGE}}$ and $\overline{\text{MEDIUM MESSAGE}}$.

(a) Long test message - The long test message is programmed into the first 96 addresses. $\overline{\text{SHORT MESSAGE}}$ and $\overline{\text{MEDIUM MESSAGE}}$ are held high, IC6/8 and IC1/8 are held low and IC7/11, IC7/3, IC7/6 and IC7/8 are enabled.

The character counter is clocked at character rate by SLAVE on pin 12 and the ROMs are addressed sequentially to generate characters from addresses 0 to 95.

The outputs appear on U1 to U7 provided that keys are not selected.

Output $O_4$ on IC8 goes high when the last character of the message is generated and, since CODER is high, IC10/6 goes low and bistable IC9/12:IC9/6 is reset with IC9/12 high. Since IC9/12 is high the character counter is reset to the 'all 0's' state.

(b) Medium test message - The medium test message is programmed into the 96th to 119th addresses. $\overline{\text{MEDIUM MESSAGE}}$ is held low. IC1/8 is high, IC7/6 and IC7/8 are held high, holding inputs A5 and A6 of the ROM high.

Thus addresses 96 to 119 of the 128 character block are addressed in sequence.

As for the long test message, LAST CHARACTER goes high at the end of the message and resets the counter.

(c) Short test message - The short test message is programmed into addresses 120 to 127. $\overline{\text{SHORT MESSAGE}}$ is held low, IC6/8 and IC1/8 are high and IC7/11, IC7/3, 6 and 8 are held high.

IC2 of the character counter thus sequences the last eight addresses of the block.

The last character resets the character counter as for the long test message.

### 3.10.1.4 Generation of a Test Message

The sequence for generating test messages is similar for all types except for the mode of addressing. As an example the sequence for a long, 5-level message is described.

The initial conditions are:-

(i) $\overline{\text{KEYS}}$ is high enabling IC3 and IC8.

(ii) $\overline{\text{SHORT MESSAGE}}$ and $\overline{\text{MEDIUM MESSAGE}}$ are high permitting IC2 and IC4 to address IC3 and IC8 directly.

(iii) $\overline{\text{8L}}$ is high selecting the 5-unit 128-character block.

(iv) Bistable IC9/12:IC9/6 is reset with IC9/12 high holding IC3 and IC4 reset.

When RUN is selected $\overline{\text{RUN}}$ goes low and $\overline{\text{SM}}$ goes high. The first character stored in the 5-level section of the ROM's is written into the serialiser and sent to line.

At the start of the first transmitted character CP goes high. CP, gated with RUN and KEYS, causes IC1/11 to go low setting bistable IC9/12:IC9/6 (with IC9/12 low and IC9/6 high) to enable the character counter IC2 and IC4. During the stop element of the first character SLAVE goes high and clocks IC3 to the second count. The second character is written into the serialiser and sent to line.

The second character SLAVE pulse steps the character counter to the third count and the sequence is repeated until the last character is addressed. During the time that the last character is presented to the serialiser via outputs U1 to U7 output $O_4$ of IC8 is high.

CODER is a high-going pulse which occurs during the last marking element of a character so that IC10/6 pulses low, resetting bistable IC9/12:IC9/6. The character counter is reset to count 0 and the test message is repeated.

This sequence continues until STOP is selected and $\overline{\text{RUN}}$ goes high.

When $\overline{\text{RUN}}$ is high $\overline{\text{SM}}$ goes low at the end of the message, when IC9/12 goes high and transmission is stopped.

During a single message $\overline{\text{RUN}}$ is taken low to start transmission and then taken high to select STOP. As before, at the end of the message $\overline{\text{SM}}$ goes low to stop transmission.

3.10.1.5 Keys

When keys are selected $\overline{\text{KEYS}}$ goes low, IC6/5 goes high and the ROM's are disabled. Inputs KEY 1 to KEY 7 set the character to be transmitted.

When $\overline{\text{KEYS}}$ goes low bistable IC9/12:IC9/6 is reset and the character counter is inhibited.

When a test message is selected the keys are disabled, $\overline{\text{KEYS}}$ is high and the character counter is freed.

3.10.2 Read-Only Memory Programming Information

3.10.2.1 Message Location

(a) Address identification

The 256 possible addresses are allocated word numbers from 0 to 255.

3.10.2.1 Message Location (Continued)

For example:

| | ADDRESS BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| Word 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Word 255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Where $A_0$ is the least significant bit.

(b) 8-Unit addresses

The 8-Unit test messages are programmed from word 0 to word 127 inclusive.

The characters of the test messages must be programmed as follows:-

| MESSAGE TYPE | FIRST CHARACTER | LAST CHARACTER |
|---|---|---|
| LONG | WORD 0 | AT OR BEFORE WORD 95 |
| MEDIUM | WORD 96 | AT OR BEFORE WORD 119 |
| SHORT | WORD 120 | AT OR BEFORE WORD 127 |

(c) 5-Unit addresses

The 5-unit messages are programmed from words 128 to 255 inclusive. The characters of the test messages must be programmed as follows:-

| MESSAGE TYPE | FIRST CHARACTER | LAST CHARACTER |
|---|---|---|
| LONG | WORD 128 | AT OR BEFORE WORD 223 |
| MEDIUM | WORD 224 | AT OR BEFORE WORD 247 |
| SHORT | WORD 248 | AT OR BEFORE WORD 255 |

3.10.2.2 R.O.M. Outputs

The ROM outputs are programmed to give logic '0' for a Mark and logic '1' for a Space.

3.10.2.2 R.O.M. Outputs (Continued)

IC3 must be programmed for bits 1 to 4 of the character required as follows:-

| OUTPUT | $O_1$ | $O_2$ | $O_3$ | $O_4$ |
|---|---|---|---|---|
| BIT | 1 | 2 | 3 | 4 |

IC8 must be programmed for bits 5 to 7 of the characters required and for the last character identification as follows:-

| OUTPUT | $O_1$ | $O_2$ | $O_3$ | $O_4$ |
|---|---|---|---|---|
| BIT | 5 | 6 | 7 | LAST CHAR |

As an example, consider the programming for a 5-unit long test message of 96 characters where the first three characters are:-

Carriage return
Line feed
Letter shift

and the last two characters are A and Z.

| WORD NUMBER | IC3 $O_1$ | IC3 $O_2$ | IC3 $O_3$ | IC3 $O_4$ | IC8 $O_1$ | IC8 $O_2$ | IC8 $O_3$ | IC8 $O_4$ |
|---|---|---|---|---|---|---|---|---|
| 128 | 1 | 1 | 1 | 0 | 1 | X | X | 0 |
| 129 | 1 | 0 | 1 | 1 | 1 | X | X | 0 |
| 130 | 0 | 0 | 0 | 0 | 0 | X | X | 0 |
| . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . |
| 222 | 0 | 0 | 1 | 1 | 1 | X | X | 0 |
| 223 | 0 | 1 | 1 | 1 | 0 | X | X | 1 |

X may be 0 or 1.

NOTES

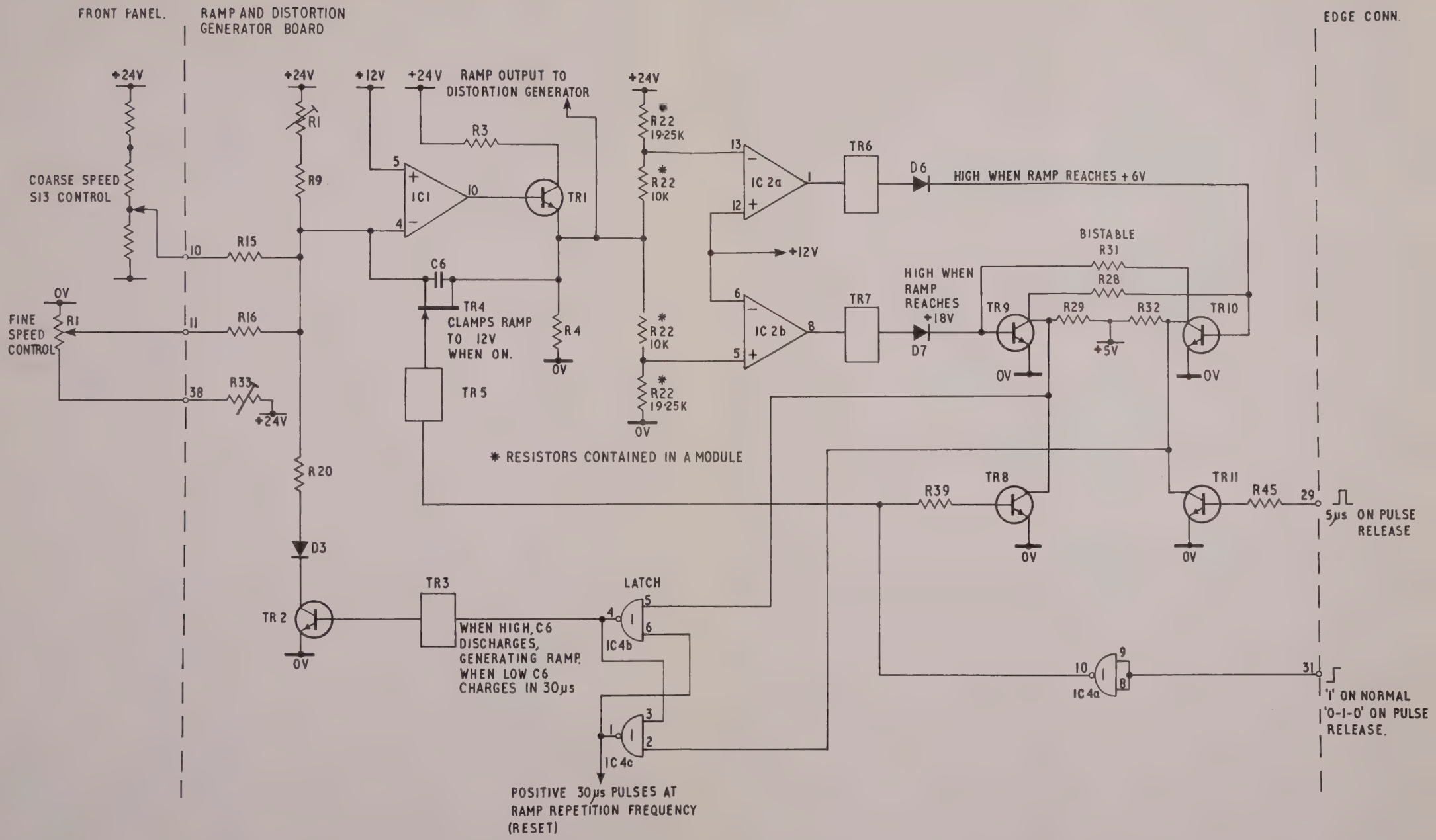
$O_2$ and $O_3$ of IC8 are specifically 0 or 1 for an 8-unit message.

$O_4$ of IC8 is always 0 except for the last character.

### 3.10.3 Serial Logic and Dry Contact Outputs

The logic circuit comprising IC11, TR1 and associated components produces identical outputs of the serial data to those described for the standard Message Generator board (see 3.7.6).

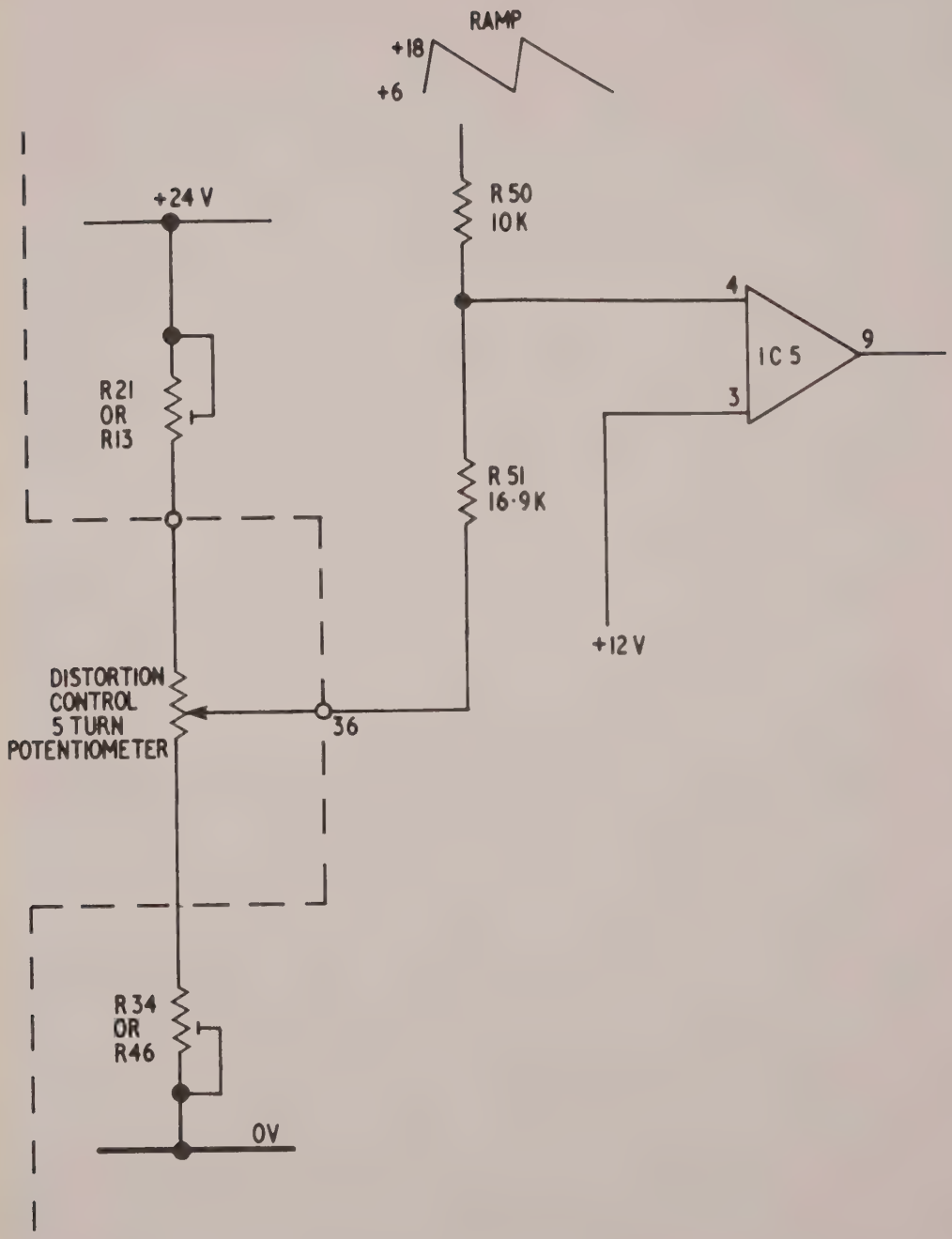
End of Section 3




SIMPLIFIED DIAGRAM OF RAMP GENERATOR.

FIG 3.1.

620/DJ/06320
SHT.7. ISS.3

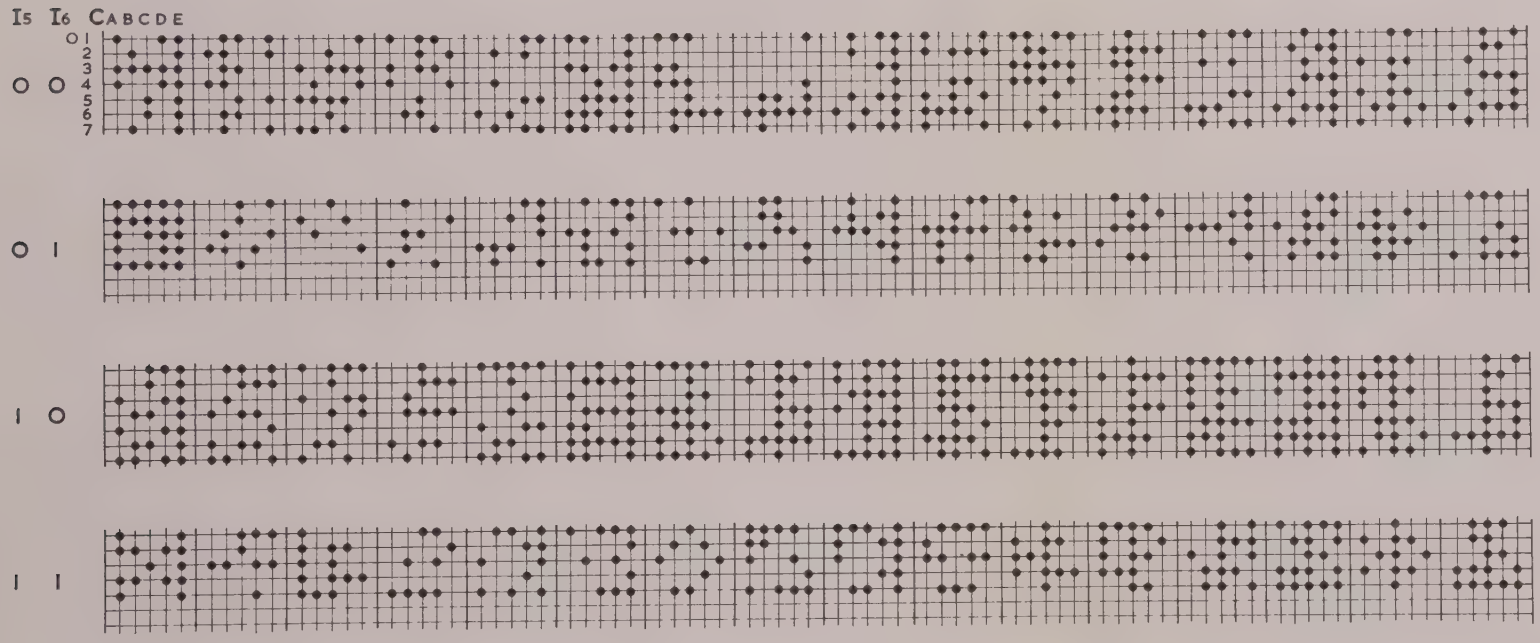



SIMPLIFIED DIAGRAM
OF DISTORTION GENERATOR FIG 3.2

## CHARACTER FORMAT

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_1$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $I_2$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| $I_3$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $I_4$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

$I_7$ POSITIVE LOGIC POLARITY

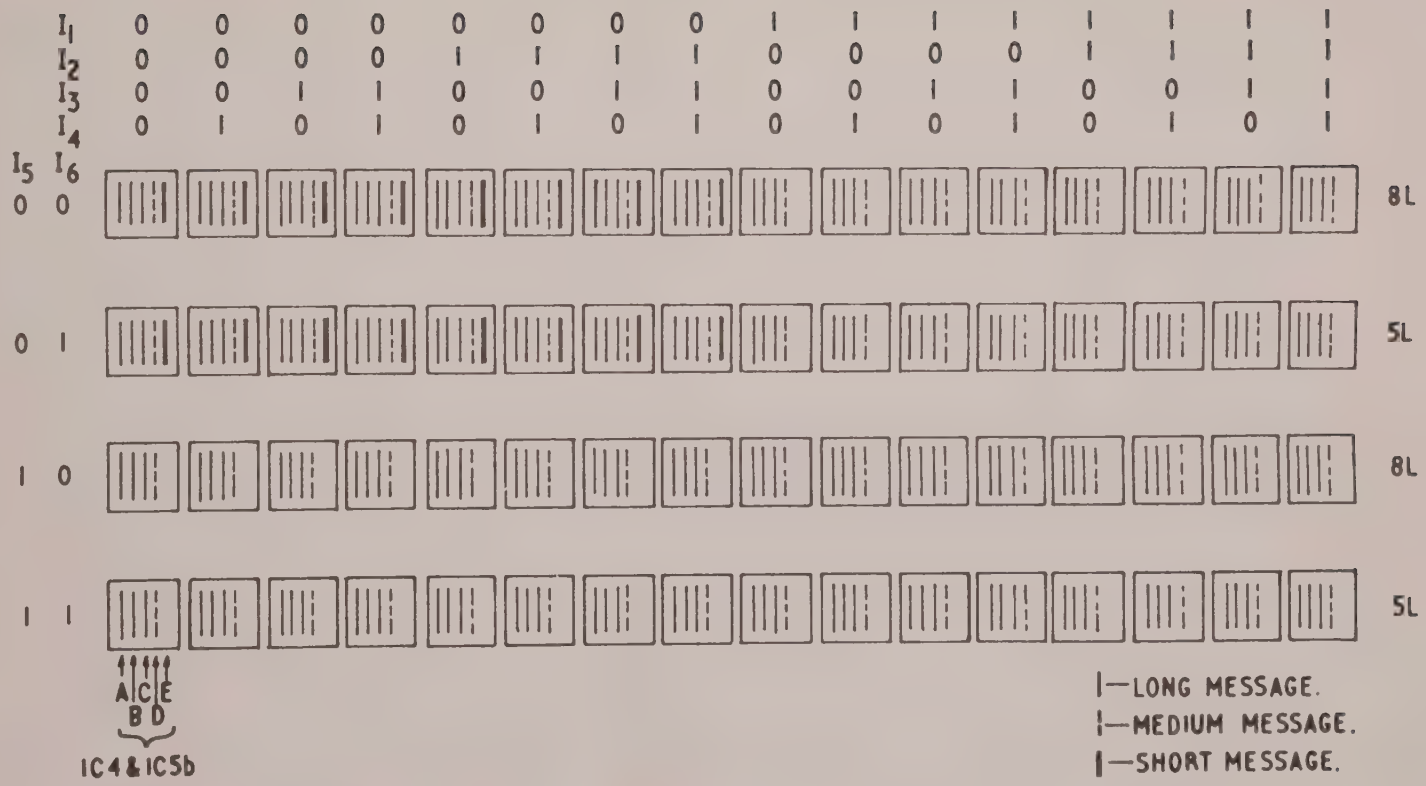



### TERMINAL ASSIGNMENTS

| PIN | | PIN | |
|---|---|---|---|
| 1 | $O_1$ | 15 | $V_{GG}$ |
| 2 | NC | 16 | $I_6$ |
| 3 | $O_2$ | 17 | $V_{SS}$ |
| 4 | NC | 18 | $C_A$ |
| 5 | $O_3$ | 19 | $C_B$ |
| 6 | NC | 20 | $C_C$ |
| 7 | $O_4$ | 21 | $C_D$ |
| 8 | NC | 22 | $C_E$ |
| 9 | $O_5$ | 23 | $I_5$ |
| 10 | NC | 24 | $I_4$ |
| 11 | $O_6$ | 25 | $I_3$ |
| 12 | NC | 26 | $I_2$ |
| 13 | $O_7$ | 27 | $I_1$ |
| 14 | $V_{DD}$ | 28 | $I_7$ |

FIG 3·3(a)

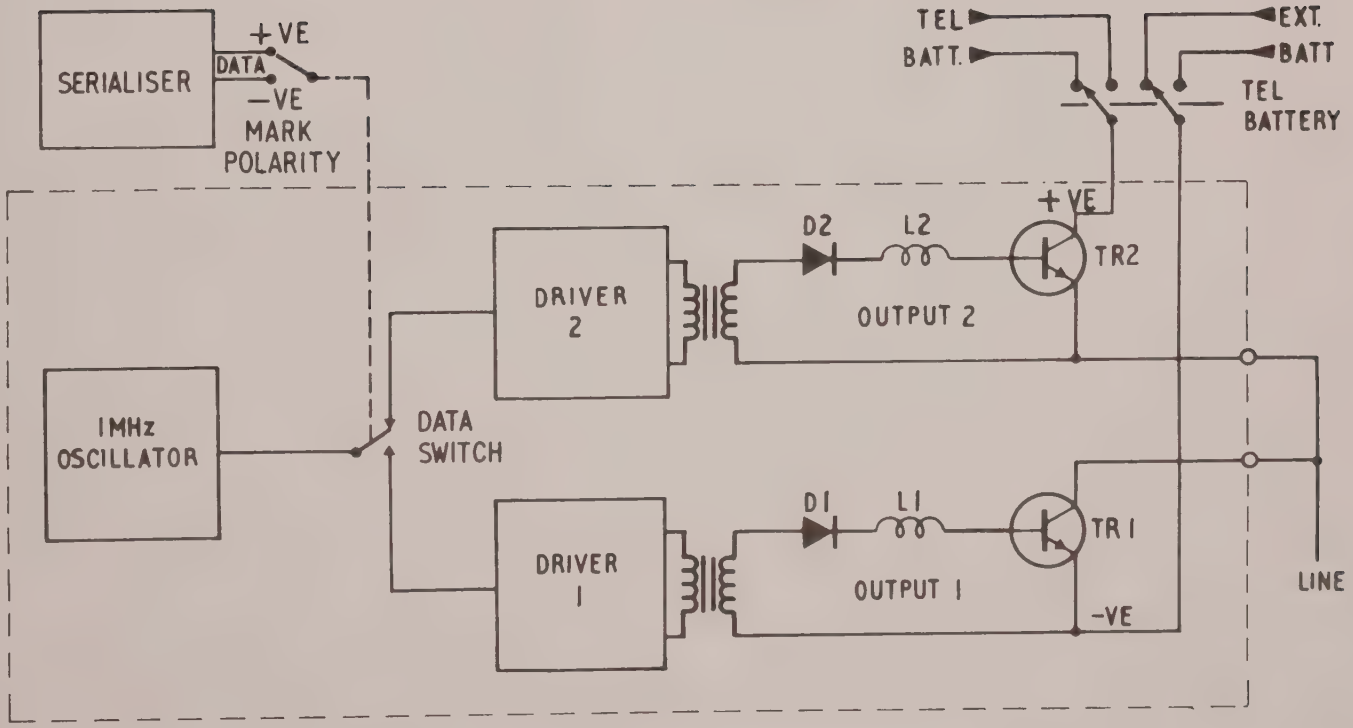
# READ ONLY MEMORY




READ-ONLY MEMORY (DATA LOCATION)

FIG 3.3 (b)

620/DJ/06320
SHT. 6. ISS. 2




BLOCK DIAGRAM ELECTRONIC OUTPUT

FIG.3.4.

620/DJ/06320
SHT.10. ISS. 3

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

## SECTION 4 - INSTALLATION

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## ILLUSTRATIONS

(at end of section)


| Figure | |
|---|---|
| 4.1. | Transformer Tappings |

# SECTION 4

# INSTALLATION

## 4.1. INSTALLATION PROCEDURE

1. Unpack the equipment and visually examine for external damage.

2. If the supply voltage to be used is within the range 195V to 255V or 97V to 127V position the voltage selector on the rear panel so that the black arrow points to the corresponding voltage marking. (The selector is a captive plug which must be pulled out to rotate). If the supply voltage to be used is outside these two ranges refer to Para. 4.2.

3. Remove the top cover, visually examine for internal damage and check that the printed circuit boards are pressed fully into their sockets.

4. If the options listed below are acceptable replace the top cover. Otherwise refer to the paragraph indicated in brackets for instructions on selecting an alternative option.

   - Release pulse polarity negative (Para. 4.3.1).
   - High internal battery supply set to 80V (Para. 4.3.2).
   - Dry contact set to on (0V) for positive mark (Para. 4.3.3).

5. Connect a suitable plug to the mains cable: Brown - Live(L), Blue - Neutral, Green/Yellow - Earth(E).

6. If adjustments have been carried out during procedure 4, replace the top cover. The instrument is now ready for operation.

## 4.2. MAINS ADJUSTMENT

If the available supply is outside the ranges obtained by means of the voltage selector the following procedure must be carried out:

(a) Remove the bottom cover to expose the transformer tapping points as shown in Figure 4.1.

(b) The following table gives details of the transformer tappings and corresponding voltage ranges.

| | Tapping Points | Range of Voltage | |
|---|---|---|---|
| | | With Voltage Selector set to 195-255 Volts | With Voltage Selector set to 97-127 Volts |
| (i) | C and G | 180 - 240 | 90 - 120 |
| (ii) | A and E | 210 - 270 | 105 - 135 |

(c) For range (i) remove wire from B and connect to C, remove wire from F and connect to G.

Similarly for range (ii) remove wire from B and connect to A, remove wire from F and connect to E.

(d) Using sticky labels note new ranges by Voltage Selector.

(e) Replace bottom cover.

## 4.3. INTERNAL ADJUSTMENTS

Three boards may require links to be altered for use with the operators equipment.

4.3.1. Release Pulse Polarity (Figure 7.4)

Normally set at the factory to -ve pulse operation. To change polarity proceed as follows:

(a) Remove the INTERFACE board, see Figure 8.3. for position.

(b) The following table gives details of the link positions required for +ve or -ve pulse operation.

| | Pulse Polarity | LINK A | LINK B | LINK C |
|---|---|---|---|---|
| (i) | + ve | open | closed | open |
| (ii) | - ve | closed | open | closed |

(c) Make the link settings as required.

4.3.2. Telegraph Battery High Voltage Links (Figure 7.1)

If a voltage other than the 80V selected in the factory is required the following procedure must be carried out:

(a) Remove the Telegraph Battery board, see Fig. 8.3 for position.

(b) Select the required high voltage level by connecting links A and B between the positive and negative link terminals and required voltage terminal. The following voltages are available:

- 80V/0V/80V
- 60V/0V/60V
- 48V/0V/48V
- 30V/0V/30V

(c) Replace the board in the correct position.

4.3.3. Message Generator Dry Contact Links (Figure 7.5)

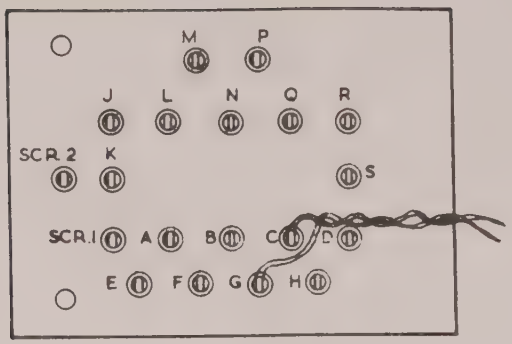
If an on (OV) dry contact output for positive mark is not acceptable the following procedure must be carried out:

(a) Remove the Message Generator board, see Figure 8.3 for location.

(b) To obtain on (OV) dry contact output for negative mark remove the link from B to C and fit across A and B.

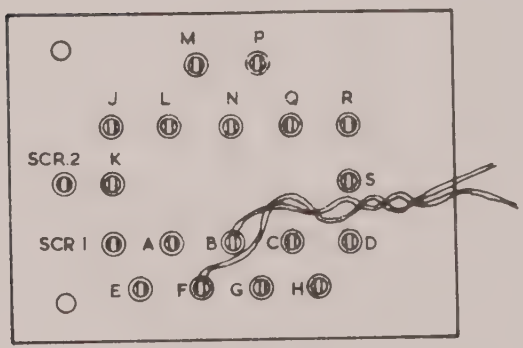
(c) Replace the board in its correct position.

End of Section 4



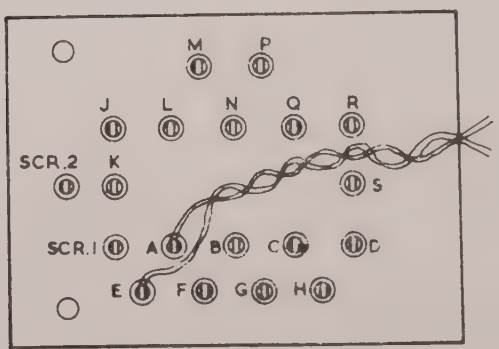

(a)

180/240V OR 90/120V OPERATION




(b)

195/255V OR 97/127 V OPERATION




(c)

210/270V OR 105/135V OPERATION

620/DJ/06320
SHT 9 ISSUE 2

TRANSFORMER TAPPINGS

FIG. 4.1

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

## SECTION 5 - OPERATION

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# SECTION 5

# OPERATION

## 5.1. INTRODUCTION

This section is divided into three parts.

(a) Details of controls - 5.2.

(b) Connections - 5.3.

(c) Operating procedure - 5.4.

All sockets and screw terminals will accept 4 mm plugs.

The equipment can be used immediately after switching on, but it is recommended that thirty minutes warming up time is allowed to achieve thermal stability.

## 5.2. CONTROLS

Reference should be made to Figures 8.1. and 8.2.

### 5.2.1. STOP ELEMENT switch (Item 1, Figure 8.1.)

(a) 5 unit code operation is selected by setting this control to a position left of vertical. 1, 1.5 or 2 stop element operation or pulsed operation may be selected.

(b) 8 unit code operation is selected by setting this control to a position right of vertical. 1, 1.5 or 2 stop element operation or pulsed operation may be selected.

5.2.2 SPEED controls (Items 2 and 3, Figure 8.1)

The SPEED controls consist of:

(a) A 12 position rotary switch with a range from 25 to 300 bauds, incrementing in 25 baud steps. It should be noted that the switch has no mechanical end stops fitted.

(b) A three turn fine SPEED potentiometer continuously variable over the range 0 to 30 bauds. Each complete turn changes the speed by 10 bauds, as shown by the white figures on the front of the control. A fine scale, calibrated in 0.1 baud steps enables the speed to be set precisely.

The speed set is the sum of the three scales, e.g.

| | | |
|---|---|---|
| Coarse control set to 125 | | 125 |
| Fine control white figures between | | |
| | 20 and 30 | 20 |
| Fine scale, black graduations | | |
| | 8.6 bauds | 8.6 |
| Speed set in bauds | | 153.6 |

When the required speed is exactly a multiple of 25 bauds it is recommended that the coarse control is set to the next lower speed and the fine control is set to 25 bauds.

When accuracy is required greater than 1% a frequency counter connected between FREQ. MON. (Item 17 Figure 8.1) and 0V (Item 16, Figure 8.1) will display twice the actual baud speed when the equipment is transmitting (not continuous MARK or continuous SPACE).

5.2.3 SIGNAL control (Item 4, Figure 8.1.)

This four position rotary switch allows the type of Test Signal to be selected:

(a) CHARACTERS - with the switch in this position the Test Signals are selected by the TEST MESSAGE/KEYS control (Item 7, Figure 8.1.). Details of this control are given in 5.2.5.

(b) MARK - a continuous MARK is transmitted, the polarity of which is selected by MARK + VE/- VE switch (Item 5, Figure 8.1.).

(c) SPACE - a continuous SPACE is transmitted the polarity of which is opposite to that selected by the MARK + VE/- VE switch.

(d) 1:1 Reversals - Alternative MARK/SPACE signals are transmitted.

NOTE: 2:2 reversals can be obtained by using the KEY switches as detailed in 5.4.

5.2.4 OUTPUT SUPPLY switch and HIGH lamp

The OUTPUT SUPPLY switch (Item 6, Fig. 8.1.) enables a variety of transmit voltages to be selected. The voltages obtained in the various switch positions are as follows:

(a) EXTERNAL - transmit voltages determined by the voltage of the external battery supply applied via the +ve and -ve battery terminals.

(b) INTERNAL: V24 - +6V and -6V with respect to TELE.

(c) INTERNAL: DOUBLE CURRENT - +High and -High with respect to TELE.

(d) INTERNAL: SINGLE CURRENT - +2 x High with respect to TELE.

The high voltage is normally 80V but voltages of 30V, 48V, or 60V can be selected by means of links on the Telegraph Battery board. With DOUBLE or SINGLE CURRENT selected the HIGH LED (Item 21, Fig. 8.1 lights).

5.2.5 TEST MESSAGE/KEYS switch (Item 7, Figure 8.1.)

With the OUTPUT switch set to CHARACTERS, this switch is set to select one of the following:

(a) SHORT Test Message

(b) MEDIUM Test Message

(c) LONG Test Message

(d) KEYS.

For details of the Test Messages see Figure 8.4. and for KEYS see 5.2.6.

5.2.6 KEYS and PARITY controls (Items 8 and 9, Figure 8.1.)

With the TEST MESSAGE/KEYS switch at KEYS a single character is transmitted as selected by the setting of KEYS, and the PARITY switch if necessary.

Details of the KEY settings for each character are given in Figure 8.5. in tape form. Each hole requires the appropriate KEY to be set to MARK and each blank the appropriate KEY is set to SPACE.

When 5 unit code operation is selected only the first 5 KEYS are operative.

When 8 unit code operation is selected all seven KEYS are operative and the PARITY switch must be set as required, e.g. if odd parity is required the PARITY switch is set to ODD and the eighth bit is automatically inserted, of the correct binary level to generate odd parity.

5.2.7. RUN/STOP switch (Item 10, Figure 8.1.)

This switch controls transmission of Test Messages and Keyed Characters.

5.2.7 RUN/STOP switch (Continued)

When set to RUN transmission is continuous. When set to STOP transmission is terminated only when the complete message or keyed character has been transmitted.

5.2.8 DISTORTION and PERCENTAGE controls

(Items 13 and 14, Figure 8.1)

The DISTORTION switch allows selection of the following types of distortion:

(a) MARK BIAS - Increases the duration of all MARK elements and correspondingly reduces the duration of all SPACE elements.

(b) SPACE BIAS - Increases the duration of all SPACE elements and correspondingly reduces the duration of all MARK elements.

(c) LONG START - Increases the duration of the Start element and correspondingly reduces the duration of the Stop element.

(d) SHORT START - Decreases the duration of the START element and correspondingly increases the duration of the Stop element.

The PERCENTAGE control is a five turn potentiometer continuously variable over the range 0 to 50%. Each complete turn changes the amount of distortion by 10% as shown by the white figures on the front of the control. A fine scale calibrated in 0.1% steps enables distortion to be set precisely.

5.2.8 DISTORTION and PERCENTAGE controls (Continued)

The Distortion set is the sum of the two scale readings, e.g.

| | |
|---|---|
| White figures between 20 and 30 | 20% |
| Fine scale, black graduations 7.5 | 7.5% |
| Distortion set | 27.5% |

5.2.9 Pulsed operation controls (Items 11 and 19, Figure 8.1.)

The STEP button (Item 11) allows the operator to transmit one character per button operation when STOP ELEMENT switch is at PULSED and RUN/STOP switch is at RUN. The character is transmitted on pressing the button which must be released before operating again to transmit the subsequent character.

The equipment can also be triggered by a suitable external source, the pulse amplitude being between 6V and 200V and connected between PULSE IN, (Item 19, Figure 8.1.) and OV (Item 16, Figure 8.1.). STOP ELEMENT must be at PULSED and RUN/STOP switches at RUN for a character to be transmitted when a pulse is received.

5.2.10 Signal output terminals (Item 20, Figure 8.1.)

Two screw terminals, LINE and TEL. E are provided to connect the equipment to the load.

5.2.11 Serial Data Terminals (Item 15, Figure 8.1.)

A Transistor Logic Level (nominal 0.8V low and 3.3V high), version of the data transmitted is available across sockets TTL Logic and OV for application to other equipment if required.

5.2.12 TRIG OUT socket (Item 18, Figure 8.1.)

This socket provides a positive going 3V pulse at the commencement of each transmitted character. The main use of this output is to externally trigger the TDMS 80.2 when used in conjunction with this equipment.

5.2.13 Mains SUPPLY switch (Item 12, Figure 8.1.)

This switch controls the mains supply and when ON the associated red indicator is illuminated.

5.2.14 VOLTAGE SELECTOR (Item 3, Figure 8.2.)

The voltage selector consists of a rotary captive plug.
To change the range pull out the captive plug, rotate it so that the black arrow points to the required range and push the plug fully in. Protection is supplied by the two fuses SUPPLY (Item 1 in Figure 8.2.) mounted on the rear panel.

The left hand fuse, 250mA, is associated with 195-255 volt range.

The right hand fuse, 500mA, is associated with 97-127 volt range.

5.2.15 Tag Block TB2 (Item 4, Figure 8.2.)

Tag block TB2 on the back panel provides screw terminals for the following signals:

(a) +ve/-ve - Provided to connect an external battery supply to the instrument.

(b) LINE/TELE - Serial data as fed to the equipment under test. Identical signals to those obtained at item 20 on the front panel.

(c) Trig Out, Pulse On, Monitor, Logic O/P - Alternative connections for signals also available at the front panel.

(d) DRY CONTACT - Dry contact version (OV Mark/Open Circuit Space) of serial data applied to equipment under test. OV output for +ve or -ve mark is selected by means of links. (Para 4.3.3.)

5.2.16 DATA O/P socket (Item 5, Figure 8.2.)

The transmitted characters are available in parallel form at this socket on the rear panel. These outputs are only usuable with equipments whose inputs are conpatible with 74 Series T.T.L. outputs.

5.2.16 DATA O/P socket (Item 5, Figure 8.2.) continued.

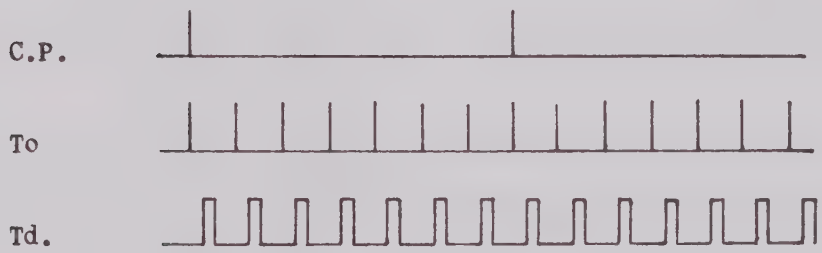
Also available at the socket are the following pulses:

(a) CHARACTER PRESET - (CP) - This is generated when the data is all present at the socket and is used to strobe the data out.

(b) To - This occurs at element rate at the start of each undistorted element.

(c) Td - This occurs at element rate at the start of each distorted element.

The relationship between C.P., To and Td are shown in the following waveforms for 5 unit code, 1 unit stop, with Td 25% distortion.




Waveforms Figure 5.1

The following table shows the pin numbers of the socket with reference to the data available:

5.2.16. DATA O/P socket (Continued)

| Pin No. | Output |
|---|---|
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 |
| 8 | 0 Volts |

| Pin No. | Output |
|---|---|
| 9 | To |
| 10 | Td |
| 11 | Not connected |
| 12 | Not connected |
| 13 | Not connected |
| 14 | Not connected |
| 15 | C.P. |

NOTE: Bit 8, the Parity bit, is not available at this socket.

5.2.17. Mains Supply Cable (Item 6, Figure 8.2.)

The cable is 2m (6' 6") in length.

## 5.3 CONNECTIONS

### 5.3.1 Introduction

This sub-section describes the connections to be made for the available facilities.

### 5.3.2 Double Current Operation

Three methods of double current operation are available:

(a) Using the internal battery supply to obtain a 6-0-6V double current signal.

(b) Using the internal battery to obtain a High-0-High double current signal.

(c) Using an external battery.

#### 5.3.2.1 Internal 6-0-6 Signal

Set the OUTPUT SUPPLY switch to INTERNAL-V24 and the MARK switch to obtain the required mark polarity.

#### 5.3.2.2 Internal High-0-High Signal

Set the OUTPUT SUPPLY switch to INTERNAL-DOUBLE CURRENT and the MARK switch to obtain the required mark polarity. Any of the following signal levels can be obtained depending on the links fitted on the Telegraph Battery board (see Para 4.3.2): 80-0-80V, 60-0-60V, 48-0-48V and 30-0-30V.

#### 5.3.2.3 External Battery

Set the OUTPUT SUPPLY switch to EXTERNAL and connect the double current battery supply to the +ve/-ve and TELE terminals at TB2 on the back panel as shown in Figure 5.2. Set the MARK switch to obtain the required mark polarity. If the polarity of the external battery supply is incorrect the EXT TEL BATTERY fuses blow.

### 5.3.3 Single Current Operation

Three methods of single current operations are available:

(a) Using the internal battery supply to obtain a 2 x +High voltage.

(b) Using an external battery to obtain a positive voltage.

(c) Using an external battery to obtain a negative voltage.

5.3.3.1 Internal 2 x +High Voltage

Set the OUTPUT SUPPLY switch to INTERNAL - SINGLE CURRENT and the MARK switch to +VE. The signal voltage is +2 times the selected high voltage for a mark and OV (open circuit) for a space. With -VE MARK selected the reverse applies.

5.3.3.2 External Positive Voltage

Set the OUTPUT SUPPLY switch to EXTERNAL and connect the external battery as shown on Figure 5.2c. Set the MARK switch to +VE. If the polarity of the external battery supply is incorrect the associated EXT TEL BATTERY fuse blows.

5.3.3.3 External Negative Voltage

Set the OUTPUT SUPPLY switch to EXTERNAL and connect the single current battery supply as shown on Figure 5.2(b). Set the MARK switch to -VE. If the polarity of the external battery supply is incorrect the associated EXT TEL BATTERY fuse blows.

5.3.4 Speed Monitoring

Connect a frequency counter across FREQ. MON and OV. The counter reading will be twice the baud speed of transmission when the equipment is transmitting (not continuous MARK or continuous SPACE).

5.3.5 External pulse connections

If an external source is to be used to pulse operate the equipment, it must be connected between PULSE IN and OV. The pulse amplitude must be between 6 and 200V. For the polarity setting see 4.3.1.

5.3.6 Triggering external equipment

If another equipment requires a synchronising pulse at the start of each transmitted character, the TRIG OUT socket supplies a positive going 3V pulse at the start of the Start element. The earth return is via OV.

5.3.7 Rack or Console mount equipments

The connections details above can be made via the Tag Block mounted on the rear panel.

5.3.8 Logic Output of Serial Data

A TTL logic level output of serial data is available across terminals TTL LOGIC/OV on the front panel or at the corresponding terminals on TB2 on the back panel.

5.3.9 Dry Contact Output

A dry contact output (OV for mark) is available across terminals DRY CONTACT/OV ot TB2 on the back panel. Different links must be fitted on the Message Generator board to obtain a OV output for positive and negative mark (see Para 4.3.3).

## 5.4 OPERATING PROCEDURE

In the early stages, until complete familiarity with the equipment is achieved, it is recommended that the operator follows the procedure below. It is assumes that all necessary external connections to the TSG 40.2 have been made in accordance with sub-section 5.3.

### 5.4.1 Initial Control Settings

(a) Set SIGNAL to MARK.

(b) Set the OUTPUT SUPPLY and MARK switched to the required positions (5.3.2 and 5.3.3).

(c) Set STOP ELEMENT to desired position (5.2.1).

(d) Using the Fine and Coarse SPEED BAUD controls set the desired speed. (5.2.2).

(e) Set STOP/RUN to STOP.

(f) Set DISTORTION to OFF.

(g) Set mains SUPPLY to ON. Check indicator illuminates and allow thirty minutes warming up time.

The equipment is now ready to transmit undistorted signals.

### 5.4.2 Selection of operating mode

#### 5.4.2.1 Free running

(a) Adjust controls to give the required Test Signals (5.4.3).

(b) Set STOP ELEMENT as required. (5.2.1).

(c) Set RUN/STOP to RUN. (5.2.7).

#### 5.4.2.2 Pulsed

(a) Adjust controls to give the required Test Signals (5.4.3).

(b) Set STOP ELEMENT to the appropriate PULSED position (5.2.1).

(c) Set RUN/STOP to RUN (5.2.7).

5.4.3 Selection of Test Signals

5.4.3.1 Characters

(a) Set SIGNAL to CHARACTERS.

(b) Set TEST MESSAGE/KEYS to KEYS.

(c) Set desired Character up on KEYS (5.2.6 and Figure 8.5).

(d) Proceed as required in 5.4.2.

5.4.3.2 Test Messages

(a) Set SIGNAL to CHARACTERS.

(b) Set TEST MESSAGE/KEYS to required Test Message - LONG, MEDIUM or SHORT (5.2.5 and Figure 8.4).

(c) Proceed as required in 5.4.2.

5.4.4 Distorting the Test Signals

Distortion can be applied to the Test Signals at any time as detailed below. Details of the control settings are given in 5.2.8.

5.4.4.1 MARK or SPACE BIAS

(a) Set DISTORTION to required bias.

(b) Set PERCENTAGE to required amount of distortion.

5.4.4.2 LONG or SHORT START

(a) Set DISTORTION to required Start length.

(b) Set PERCENTAGE to required amount of distortion.

5.4.5 Selection of Continuous MARK or SPACE Signals

(a) Set SIGNAL to required signal, MARK or SPACE (5.2.3).

(b) Proceed as required in 5.4.2.

5.4.6 Selection of 1:1 or 2:2 Reversals

5.4.6.1 1:1 Reversals

(a) Set SIGNAL to 1:1.

(b) Proceed as required in 5.4.2.

5.4.6.2 1:1 Reversals - Distortion Required

(a) Set SIGNAL to CHARACTERS.

(b) Set TEST MESSAGE/KEYS to KEYS.

(c) Set STOP ELEMENT to 8 level CODE, 1 unit STOP.

(d) Set KEYS as follows:

| KEY | 1 | 2 | 3 | 4 | 5 | 6 | 7 | PARITY |
|---|---|---|---|---|---|---|---|---|
| | M | S | M | S | M | S | M | EVEN |

(e) Proceed as required in 5.4.2.

5.4.6.3 2:2 Reversals

(a) Set SIGNAL to CHARACTERS.

(b) Set TEST MESSAGE/KEYS to KEYS.

(c) Set STOP ELEMENT to 2 on 5 UNIT CODE.

(d) Set KEYS as follows:

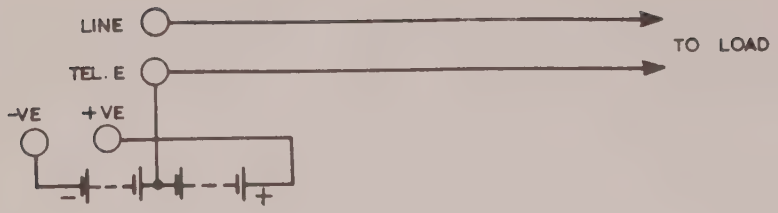
| KEY | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| SETTING | S | M | M | S | S |

(e) Proceed as required in 5.4.2.

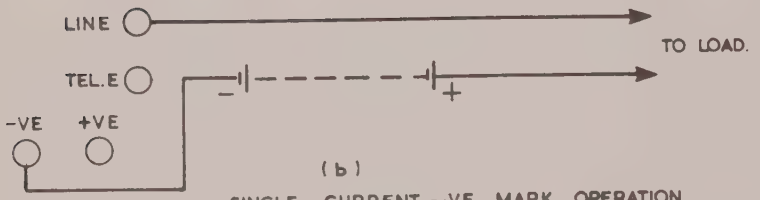
5.4.7 To Stop Transmitting

Set STOP/RUN to STOP (5.2.7).

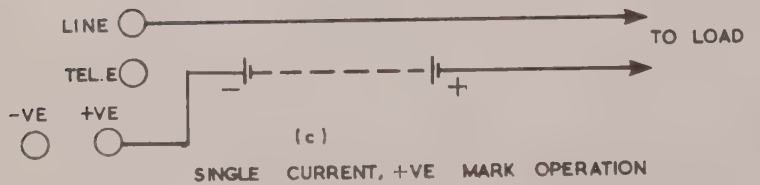
End of Section 5




(a)
DOUBLE CURRENT OPERATION




(b)
SINGLE CURRENT, -VE MARK OPERATION




(c)
SINGLE CURRENT, +VE MARK OPERATION

EXTERNAL TELEGRAPH BATTERY

FIG. 5·2

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

## SECTION 6 - MAINTENANCE

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# SECTION 6

## MAINTENANCE

### 6.1 GENERAL

This section covers:

(a) Recalibration.

(b) Functional Testing.

(c) Calibration of the Telegraph Battery Board.

Fault finding is not covered. With the assistance of Section 3 the engineer should have little difficulty in tracing a faulty component. Fault finding is facilitated by the use of an extender board, Plessey Part Number 620/2/06300. Before using the board in Socket SKB, strap SKB4 to SKB8 at the back of the socket (if they are not already permanently wired) and make a similar connection on the extender socket.

It is recommended that both the recalibration and the Functional tests are carried out at least every three months. This period may be shortened in view of experience and the degree of accuracy required.

The order in which the recalibration and functional tests are given must be strictly followed.

**WARNING**

**LETHAL VOLTAGES ARE EXPOSED WHEN EITHER THE TOP OR BOTTOM COVERS ARE REMOVED. EXTREME CARE MUST BE TAKEN WHEN TESTING THE EQUIPMENT WITH THESE COVERS REMOVED.**

## 6.2. TEST GEAR

Listed below is the test gear required together with suitable examples where necessary.

For recalibration the following are required:

(a) One voltmeter - AVO 8.

(b) One general purpose single-beam oscilloscope - Philips PM 3230.

(c) One four digit counter - RACAL SA 535B.

(d) One small screwdriver.

For the functional tests the following are required:

(a) One general purpose single beam oscilloscope - Philips PM 3230.

(b) One pulse generator - Venner TSA 628.

(c) One 5 level Teleprinter - Teletype Type 32.

(d) One 8 level Teleprinter - Teletype Type 33.

(e) One suitable battery for external use.

## 6.3. PREPARATION FOR RECALIBRATION

(a) Disconnect the TSG 40.2 from the mains. Remove the top and bottom covers. Read the WARNING at the end of 6.1. Connect the equipment to the mains and switch on.

6.3. PREPARATION FOR RECALIBRATION (Continued)

(b) The recalibration should be carried out in an ambient temperature between 20°C and 35°C. Leave the equipment switched on for 30 minutes to warm up prior to the test.

(c) Connect the digital counter to the mains, switch on and allow 30 minutes warming up time.

6.4. SETTING UP THE POWER SUPPLY

Refer to Figure 8.3. for the position of the Power Supply Unit board. The potentiometers mentioned in this sub-section are mounted on this board and can be adjusted with the board in situ.

1. Set the voltmeter to measure 24V d.c. Connect to:

   (a) SK F pin 2; 0V.

   (b) SK F pin 1; nominally + 24V.

2. If necessary adjust R1 for a reading of exactly +24V.

3. Connect the positive probe to SK F pin 14; nominally + 5V.

4. If necessary adjust R17 for a reading of exactly +5V.

5. Disconnect the voltmeter. The Power Supply Unit is now set up.

6.5. CALIBRATION OF THE OSCILLATOR

Refer to Figure 8.3. for the position of the Ramp Generator Board. The potentiometers mentioned in this subsection are mounted on this board and can be adjusted with the board in situ.

6.5 CALIBRATION OF THE OSCILLATOR (Continued)

1. Connect the counter to the FREQ MON and OV sockets on the front panel.

2. Set SIGNAL to 1:1 reversals.

3. Set the counter to measure the duration of 100 periods. Set the counter to display time periods of 1mS.

4. (a) SPEED switch to 25 Bauds.

   (b) SPEED potentiometer to 0 Bauds.

5. Check the counter reads between 1998 and 2002 mS.

6. If the reading is not within tolerance adjust R1 to bring the reading to 2000mS.

7. Set SPEED switch to 150 Bauds. Change counter range to 100uS time periods.

8. Check the counter reads between 333.0 and 333.7mS.

9. If the reading is not within tolerance adjust R2 to bring the reading to 333.3.

10. If alteration of R1 or R2 has been necessary repeat 3 to 9 until the readings in 5 and 8 are both within tolerance.

11. Set:

    (a) SPEED switch to 25 Bauds.

    (b) SPEED potentiometer to 25 Bauds.

6.5. CALIBRATION OF THE OSCILLATOR (Continued)

12. Check the counter reads between 999.0 and 1001mS.

13. If the reading is not within tolerance adjust R33 to bring the reading to 1000mS.

14. Set the SPEED potentiometer to 0 Bauds.

15. Set the SPEED switch to each position listed in the following table. Check that the counter reading is within the figures given.

| SPEED switch setting - Bauds | COUNTER reading m/s | |
|---|---|---|
| | Lower limit | Upper limit |
| 25 | 1998 | 2002 |
| 50 | 998.0 | 1002 |
| 75 | 665.4 | 668.0 |
| 100 | 499.0 | 501.0 |
| 125 | 399.2 | 400.8 |
| 150 | 332.7 | 334.0 |
| 175 | 285.1 | 286.3 |
| 200 | 249.5 | 250.5 |
| 225 | 221.7 | 222.7 |
| 250 | 199.6 | 200.4 |
| 275 | 181.4 | 182.2 |
| 300 | 166.3 | 167.0 |

If a reading is outside the tolerance the resistors associated with S13, Figure 8.6, must be checked, and replaced as necessary. The resistors are marked with their value.

6.5 CALIBRATION OF THE OSCILLATOR (Continued)

15. Continued

After replacement of a resistor the above test must be repeated.

16. When the test in 15 is satisfactory calibration of the Oscillator is complete.

6.6 DISTORTION POTENTIOMETER CALIBRATION

Refer to Figure 8.3 for the position of the Ramp Generator board. The potentiometers mentioned in this subsection are mounted on this board and can be adjusted in situ.

1. Connect the oscilloscope to SK E pin 30 and pins 2 (0V). The TRIG OUT socket may be used to obtain synchrony.

2. Set the DISTORTION switch to LONG START.

3. Set the DISTORTION potentiometer to 0%.

4. Adjust R46 to obtain a negative pulse of minimum duration. Do not remove the pulse altogether.

5. Set the DISTORTION potentiometer to 50%.

6. Adjust R13 to obtain a positive pulse of minimum duration. Do not remove the pulse altogether.

7. Repeat 3 to 6 until no further adjustments on the potentiometers are required when the DISTORTION potentiometer is moved between 0% and 50%.

## 6.6 DISTORTION POTENTIOMETER CALIBRATION

8. Set the DISTORTION switch to SHORT START.

9. Set the DISTORTION potentiometer to 0%.

10. Adjust R21 to obtain a positive pulse of minimum duration. Do not remove the pulse altogether.

11. Set the DISTORTION potentiometer to 50%.

12. Adjust R34 to obtain a negative pulse of minimum duration. Do not remove the pulse altogether.

13. Repeat 9 to 12 until no further adjustment of the potentiometers are required when the DISTORTION potentiometer is moved between 0% and 50%.

14. Calibration of the DISTORTION potentiometer is now complete.

## 6.7 COMPLETION OF CALIBRATION

When the Calibration procedure detailed in the preceding subsections has been satisfactorily completed:

1. Disconnect the Test Gear.

2. Switch off and disconnect the Mains supply.

3. Replace the top and bottom covers.

4. Re-connect the Mains supply and switch on.

The equipment is now ready for the Functional Test.

## 6.8. FUNCTIONAL TEST

### 6.8.1. General

The Functional Test may be carried out without Calibration having been checked. In this case the equipment should be allowed to reach operating temperature before carrying out the Functional Test.

If any test fails fault finding and correction should be carried out and the test repeated before proceeding to the next test.

### 6.8.2. Tests

1. Connect the oscilloscope between LINE and TEL.E. Switch on the oscilloscope. The TRIG OUT socket provides signals for obtaining synchrony.

2. Connect the Pulse Generator between PULSE IN and 0V. See section 5.3.5. Do NOT switch on the Pulse Generator.

3. Connect the external battery to +VE and -VE terminals.

4. Set:

   (a) SPEED controls for 165 Bauds.

   (b) OUTPUT SUPPLY to EXTERNAL

   (c) SIGNAL switch to 1:1.

5. Obtain a stable display on the oscilloscope. Check that the output is substantially symmetrical with an amplitude equivalent to the voltage of the External Battery.

6. Set OUTPUT SUPPLY to the various internal positions in turn and check the voltages:

6.8.2. Tests (Continued)

6. Continued.

(a) V24 - +6V/0V/-6V

(b) DOUBLE CURRENT - +High V/0V/-High V

(c) SINGLE CURRENT - +2 x High V/0V

7. Set:

(a) SIGNAL to SPACE.

(b) MARK POLARITY to +VE.

8. Check that the output is a negative d.c. condition.

9. Set MARK POLARITY to -VE.

10. Check that the output is a positive d.c. condition.

11. Set SIGNAL to MARK.

12. Check that the output is a negative d.c. condition.

13. Set:

(a) SIGNAL to CHARACTERS.

(b) DISTORTION to OFF.

(c) TEST MESSAGE/KEYS to KEYS.

(d) RUN/STOP to RUN.

(e) STOP ELEMENT to 5 level CODE, 2 unit STOP element.

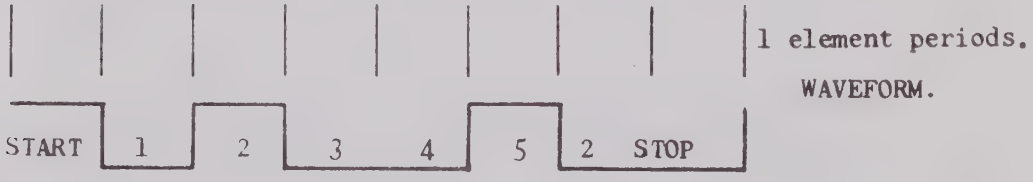
14. Set the KEYS as follows:

6.8.2. Tests (Continued)

14. Continued.

| KEY | SETTING |
|---|---|
| 1 | MARK |
| 2 | SPACE |
| 3 | MARK |
| 4 | MARK |
| 5 | SPACE |
| 6 and 7 | Immaterial |

15. Obtain a stable display and adjust the oscilloscope controls so that only one complete character is displayed as shown below.




Check that the waveform is correct.

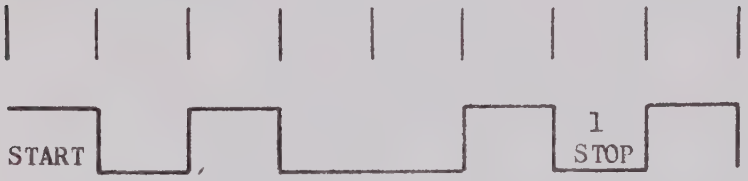
16. Set STOP ELEMENT to 5 level CODE, 1.5 unit STOP element. Do not adjust oscilloscope controls.

17. Check that the display is as shown below.

6.8.2. Tests (Continued)

18. Set STOP ELEMENT to 5 level CODE, 1 unit STOP element. Do not adjust oscilloscope controls.

19. Check that the display is as shown below.




20. Set RUN/STOP to STOP. Check that transmission ceases.

21. Set RUN/STOP to RUN. Check transmission occurs.

22. Set STOP ELEMENT to 5 level CODE, PULSED. Check transmission ceases.

23. Press the STEP button. Do not release. Check that transmission occurs. Release the STEP button. Check that no transmission occurs.

24. Press and release the STEP button. Check that only one character is transmitted each time the button is pressed, i.e. the signal remains low at the end of the STOP element.

25. Switch on the Pulse Generator. Set the Pulse Recurrence frequency to < 10 p.p.s.

26. Check that only one character is transmitted per pulse, i.e. the display remains low at the end of the STOP element.

27. Switch off the Pulse Generator.

6.8.2. Tests (Continued)

28. Set:

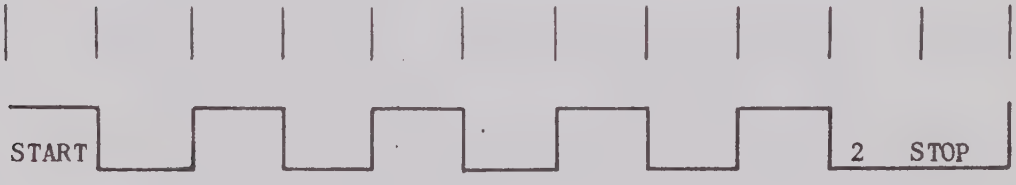
(a) STOP ELEMENT to 8 level CODE, 2 unit STOP element.

(b) PARITY to EVEN.

29. Set the KEYS as follows.

| KEY | SETTING |
|---|---|
| 1 | MARK |
| 2 | SPACE |
| 3 | MARK |
| 4 | SPACE |
| 5 | MARK |
| 6 | SPACE |
| 7 | MARK |

30. Obtain a stable display and adjust the oscilloscope controls so that only one complete character is displayed as shown below.




Check that the waveform is correct.

31. Using each KEY in turn:

6.8.2. Tests (Continued)

31. Continued.

(a) Set the KEY to the opposite setting stated in the table in 29.

(b) Check the appropriate element changes state.

(c) Check the parity element changes state.

(d) Reset the KEY to the setting stated in the table in 29.

(e) Check the display is the same as in 30.

32. Ensure all the KEYS are in the position stated in the table in 29. Set PARITY to ODD. Check that the Parity element is now low.

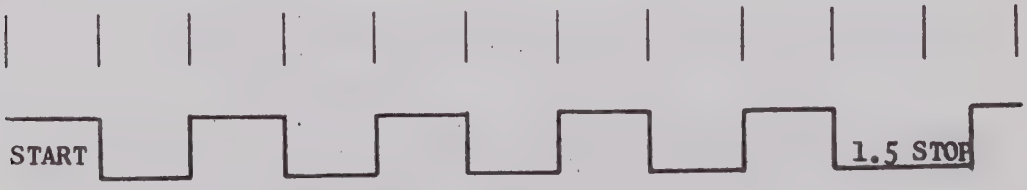
33. Set:

(a) PARITY to EVEN.

(b) STOP ELEMENT to 8 level CODE, 1.5 unit STOP element.

Do not adjust oscilloscope controls.

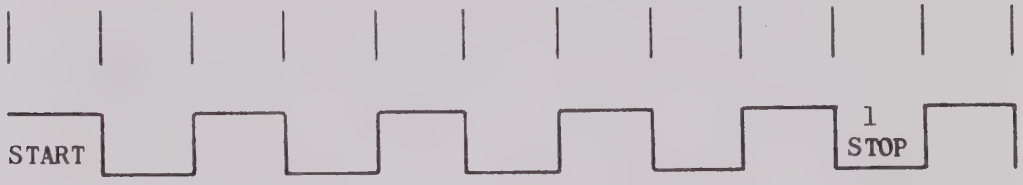
34. Check that the display is as shown below.



6.8.2. Tests (Continued)

35. Set STOP ELEMENT to 8 level CODE, 1 unit STOP element. Do not adjust oscilloscope controls.

36. Check that the display is as shown below.




37. Set STOP ELEMENT to 8 level CODE, PULSED. Check that transmission ceases.

38. Press and release the STEP button. Check that only one character is transmitted when the button is pressed i.e. the signal remains low at the end of the STOP element.

39. Set:

(a) STOP ELEMENT to 8 level CODE, 1 unit STOP element.

(b) DISTORTION switch to LONG START.

(c) DISTORTION potentiometer to 25%.

40. Check:

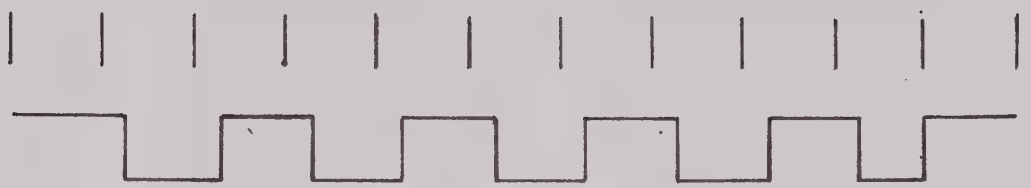
(a) the START element duration is increased by $\frac{1}{4}$ element.

(b) the STOP element duration is reduced by $\frac{1}{4}$ element.

(c) all remaining elements are of standard duration, but shifted to the right by $\frac{1}{4}$ element as shown overleaf.

6.8.2 Tests (Continued)

40. Continued.



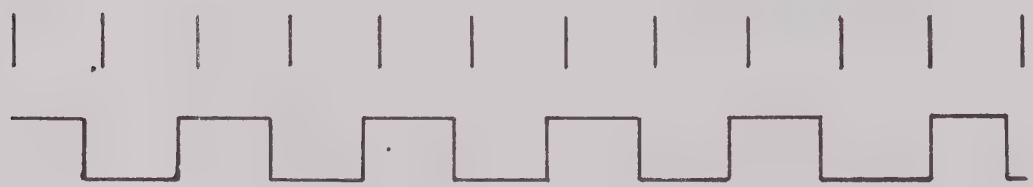
41. Set DISTORTION switch to SHORT START.

42. Check:

(a) the START element duration is reduced by $\frac{1}{4}$ element.

(b) the STOP element duration is increased by $\frac{1}{4}$ element.

(c) all remaining elements are of standard duration but shifted to the left by $\frac{1}{4}$ element as shown below.



43. Set DISTORTION switch to SPACE BIAS.

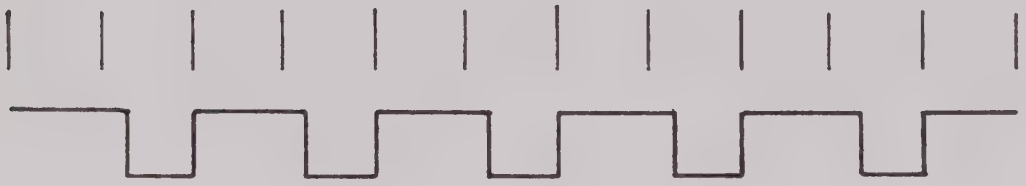
44. Check:

(a) all SPACE elements, i.e. all positive pulses, have a duration of one and one quarter standard elements.

6.8.2 Tests (Continued)

44. Continued.

(b) all MARK elements, i.e. all negative pulses, have a duration of three quarters of a standard element.



45. Set DISTORTION switch to MARK BIAS.

46. Check:

(a) all SPACE elements, i.e. all positive pulses, have a duration of three quarters of a standard pulse.

(b) all MARK elements, i.e. all negative pulses, have a duration of one and one quarter standard elements.

47. Disconnect:

(a) the Oscilloscope.

(b) the Pulse Generator.

48. Set the following controls as necessary for operation with the 5 level code Teleprinter:

(a) STOP ELEMENT

(b) SPEED

(c) MARK +VE/-VE

(d) OUTPUT SUPPLY (see 5.3.2 and 5.3.3)

6.8.2 Tests (Continued)

48. Continued

Set:

(a) DISTORTION to OFF.

(b) RUN/STOP to STOP.

49. Connect the 5 level code Teleprinter to the TSG 40.2 and switch on the Teleprinter.

50. Set:

(a) SIGNAL to CHARACTERS.

(b) TEST MESSAGE/KEYS to SHORT

(c) RUN/STOP to RUN.

51. Check for correct reception of the Test Message against Figure 8.4.

52. Whilst a Test Message is in the process of being transmitted set RUN/STOP to STOP.

Check the Test Message is completed, with no garbling of characters, before transmission ceases.

53. Set TEST MESSAGE/KEYS to MEDIUM. Repeat 51 and 52.

54. Set TEST MESSAGE/KEYS to LONG. Repeat 51 and 52.

55. Disconnect the 5 level code Teleprinter.

6.8.2. Tests (Continued)

56. Set the following controls as necessary for operation with the 8 level code Teleprinter:

(a) STOP ELEMENT

(b) SPEED

(c) PARITY

(d) MARK +VE/-VE

(e) OUTPUT SUPPLY (See 5.3.2. and 5.3.3.)

Set:

(a) DISTORTION to OFF

(b) RUN/STOP to STOP

57. Connect the 8 level code Teleprinter to the TSG 40.2 and switch on the Teleprinter.

58. Repeat 50 to 54.

59. Disconnect the 8 level code Teleprinter.

60. The functional tests are now completed.

## 6.9. TELEGRAPH BATTERY BOARD CALIBRATION

### 6.9.1. General

When new components are fitted to the diode potential divider on the Telegraph Battery board this procedure must be carried out.

6.9.1. General (Continued)

For ease of identification the link positions are numbered both in Figure 7.1., which shows the actual position on the board, and in Figure 8.7. which shows the link position in the circuit.

It is advantageous, but not essential, to use two voltmeters and an extender board for this Calibration.

The location of the board is shown in Figure 8.3.

6.9.2. Preparation

Preparation for the Calibration is detailed in 6.3.(a).

6.9.3. Calibration

Refer to Figure 8.7.

1. Measure the voltages at pins 39 and 32 with respect to edge connector pin 22.

   Pin 39 is nominally +6V to +7V

   Pin 32 is nominally -6V to -7V

2. If the voltage amplitudes are within 0.4V of each other the link connections are satisfactory.

3. If the voltage at pin 39 is greater than that at pin 32 by more than 0.4V:

   EITHER connect link 1

   OR remove link 6

6.9.3. Calibration (Continued)

3. Continued.

If the voltage at pin 39 is less than that at pin 32 by more than 0.4V:

EITHER connect link 6

OR remove link 1

Check the voltages after making the necessary alterations. They should now be within 0.4V of each other.

4. Measure the voltages at the +30V and -30V terminals with respect to edge connector pin 22. Both voltages should be within the range 29V to 33V approx.

5. If the voltage amplitudes are within 2 volts of each other the link connections are satisfactory.

6. If the difference in the voltage amplitudes is greater than 2 volts alter the link connections as necessary keeping the outputs as close to 30 volts as possible using the following information:

(a) Connecting links 2 and/or 3 decreases the positive voltage amplitude.

(b) Connecting links 7 and/or 8 decreases the negative voltage amplitude.

Check the voltages after making the necessary alterations. They should now be within 2 volts of each other.

7. Measure the voltages at the +60V and -60V terminals with respect to edge connector pin 22. Both voltages should be within the range 58V to 65V approx.

# TELEGRAPH SIGNAL GENERATOR

## TSG 40

## SECTION 7 - PARTS LIST

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# COMPONENTS LIST

Title ..... TELEGRAPH BATTERY .....

Drawing No. ..... 620/1/07097 ..... Issue No. ..... 1 .....

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1, 2 | 68 µF + 50% - 10%, 160V<br>ERIE Z1105 100-0680-0T-0161 | 402/4/55483/001 |
| DIODES | | |
| D1-4 | TRANSITRON IN647 | 415/4/98034/015 |
| D5, 6, 8, 11, 13 | ± 5%, 1.5W MULLARD BZY96 C6V2 | 415/4/98269/005 |
| D7, 9 | 1S920 | 415/4/98153/001 |
| D10, D14 | ± 5%, 0.4W MULLARD BZY88 C4V3 | 415/4/98091/009 |
| D15-20 | 20W, MULLARD BZY93 C18 | |
| D21-24 | ± 5%, 0.4W, MULLARD BZY88 C3V3 | 415/4/98091/008 |
| FUSES | | |
| FS1, 2 | 80mA, 250V BESWICK TDC13 | 518/4/98052/003 |
| RESISTORS | | |
| R1, 2 | 220, ± 5%, 3W, CGS C3A | 403/4/78355/032 |
| R3, 4 | 9.1K, ± 5%, 7W, CGS C7 | 403/4/03566/004 |
| R5, 6 | 180, ± 2% Electrosyl TR5 | 403/4/78127/431 |
| R7, R8 | 75, ± 2% Electrosyl TR5 | 403/4/78127/422 |
| TRANSISTORS | | |
| TR1 | TIP 30C and Mica Washer | 417/4/98774/003 |
| TR2 | 2N3739 | 417/4/98273/002 |

# COMPONENTS LIST

Title ..... POWER SUPPLY .....

Drawing No. ..620/1/06347..... Issue No. 9 (Sht.1) 2 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1 | 0.068µF ± 10% 100V MULLARD 344 25683 | 400/4/98785/002 |
| C2 | 470µF 25v MULLARD 017 16471 | 402/4/55475/039 |
| C3 | 2200µF 6.3V MULLARD 017 13222 | 402/4/55475/013 |
| C4 | 0.047µF ± 10% 100V MULLARD 344 25473 | 402/4/98785/001 |
| C5 | 80µF 16V MULLARD C426 AR/E80 | 402/4/55475/036 |
| DIODES | | |
| D1, 6 | MULLARD BZY88 C5V6 | 415/4/98091/003 |
| D2, 3, 4, 5. | IN 4002 | 415/4/98243/002 |
| D7 | MULLARD BZY88 C4V3 | 415/4/98091/009 |
| D8, 9, 10, 11 | 15020 | 415/4/98217/001 |
| D12 | MULLARD BZY88 C3V9 | 415/4/98091/011 |
| D13, 14. | IN 4148 | 415/4/98393/000 |
| FUSES | | |
| FS1 | 250mA BESWICK TDC13 | 518/4/98052/018 |
| FS2 | 1A BESWICK TDC13 | 518/4/98052/014 |
| POTENTIOMETERS | | |
| R1 | 470 ohms AB METALS AB83 PCH | 404/4/98214/008 |
| R17 | 1K ohms AB Metals AB83 PCH | 404/4/98214/003 |

## COMPONENTS LIST

Title ...POWER SUPPLY (Contd.).....

Drawing No. ..620/1/06347..... Issue No. 9 (Sht.1) 2 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| RESISTORS | | |
| R2 | 820 ohms ± 2% ELECTROSIL TR5 | 403/4/78127/447 |
| R3, 8, 13, 22 | 10K ohms ± 2% Electrosil TR5 | 403/4/78127/473 |
| R4, 21, 24 | 1K ohms ± 2% Electrosil TR5 | 403/4/78127/449 |
| R5 | 1.2K ohms ± 2% Electrosil TR5 | 403/4/78127/451 |
| R6 | 150 ohms ± 2% Electrosil TR5 | 403/4/78127/429 |
| R7 | 18 ohms ± 5% CGS C3A | 403/4/78355/041 |
| R9, 14 | 3.9K ohms ± 2% Electrosil TR5 | 403/4/78127/463 |
| R10 | 3.3K ohms ± 2% Electrosil TR5 | 403/4/78127/461 |
| R11 | 4.7 ohms ± 5% CGS C3A | 403/4/78355/025 |
| R12 | 220 ohms ± 2% Electrosil TR5 | 403/4/78127/433 |
| R15 | 1.8K ohms ± 2% Electrosil TR5 | 403/4/78127/455 |
| R16 | 0.27 ohms ± 5% CGS - C3A | 403/4/78355/031 |
| R18 | 100 ohms ± 2% Electrosil TR5 | 403/4/78127/425 |
| R19, 20 | 15 ohms ± 2% Electrosil TR5 | 403/4/78127/405 |
| R23 | 2.2K ohms ± 2% Electrosil TR5 | 403/4/78127/457 |
| R25 | 1.5 ohms ± 5% CGS - C3A | 403/4/78355/013 |
| R26 | 680 ohms ± 2% Electrosil TR5 | 403/4/78127/445 |
| R27 | 47 ohms ± 2% Electrosil TR5 | 403/4/78127/417 |
| TRANSISTORS | | |
| TR1, 2, 7, 8 | BC107 | 417/4/98082 |
| TR3, 9 | BCY70 | 417/4/98267/001 |
| TR4, 5, 10, 11 | BFY51 | 417/4/98085 |
| TR6 | BCY72 | 417/4/98267/003 |

## COMPONENTS LIST

Title ...RAMP AND DISTORTION GENERATORS BAUD MONITOR.....

Drawing No. ..620/1/06325..... Issue No. 15 (Sht.1) 11 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1 | 15μF − 10% + 50% 40V<br>MULLARD 01517159 | 402/4/55475/043 |
| C3 | 47pF + 20% 200V<br>ERIE N750YD | 400/4/98595/045 |
| C4,8,9,12,14-16 | 0.1μF − 25% + 50% 30V<br>ERIE 811/T/30V | 400/4/98190/051 |
| C6 | 0.125μF + 0.5% 200V<br>LEMCO MS 3000/M/R/M125D/200 | 424/4/98129/006 |
| C7, 17 | 0.22μF + 50% − 25% 6V<br>ERIE 811/T/6V | 400/4/98190/016 |
| C10 | 220pF + 20% 500V<br>ERIE N4700 801 | 400/4/98566/007 |
| C11 | 4700pF + 20% 500V<br>ERIE K170051811 | 400/4/98112/019 |
| C13 | 10,000pF + 25% 250V<br>ERIE Hi-K K750 012-BD | 400/4/98329/005 |
| DIODES | | |
| D1-7, 9-12 | IN 4148 | 415/4/98393/000 |
| D8 | ZENER MULLARD BYZ88 C6V2 | 415/4/98091 |

## COMPONENTS LIST

Title ...RAMP. AND. DISTORTION. GENERATORS,. BAUDS. MONITOR. (Contd.).....

Drawing No. ..620/1/06325..... Issue No. 15 (Sht.1) 11 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| INTEGRATED CIRCUITS | | |
| IC1 | SN72741P | 445/4/98171 |
| IC2 | SN72720N | 445/4/98112 |
| IC3 | SN72709N | 445/4/98041/004 |
| IC4 | SN7402N | 445/4/98063/003 |
| IC5 | SN72710N | 445/4/98042/004 |
| POTENTIAL DIVIDERS | | |
| R22 | MODULE | 403/4/78532 |
| POTENTIOMETERS | | |
| R1, 2. | 5K + 10%<br>AMPHENOL - BORG 2600P - 502 - 5K | 404/4/98103/009 |
| R13, 21, 34, 46 | 470 ohms + 30%<br>AB METALS TYPE 83 PCH<br>METRIC VERSION | 404/4/98214/008 |
| R33 | 200 ohms + 10%<br>AMPHENOL - BORG 2600P - 502 - 200 | 404/4/98103/005 |
| RESISTORS | | |
| R3,38 | 220 ohms + 2%<br>ELECTROSYL TR5 | 403/4/78127/433 |
| R4,12,27,30,41,<br>42,43,54. | 1K ohms + 2%<br>Electrosyl TR5 | 403/4/78127/449 |
| R5 | 3K ohms + 2%<br>Electrosyl TR5 | 403/4/78127/460 |
| R6, 37 | 47 ohms + 2%<br>Electrosyl TR5 | 403/4/78127/417 |
| R35 | 1.5K ohms + 2%<br>ELECTROSYL TR5 | 403/4/78127/453 |

## COMPONENTS LIST

Title ..... RAMP AND DISTORTION GENERATORS, BAUDS MONITOR (Contd)

Drawing No. ..... 620/1/06325 Issue No. 15.(Sht.1) 11.(Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| R9 | 102500 ± 0.1% MORGANITE FC55 | 620/4/06212 |
| R10,29,32,55 | 2.2K ohms ± 2% Electrosyl TR5 | 403/4/78127/457 |
| R11 | 22K ohms ± 2% ELECTROSYL TR5 | 403/4/78127/481 |
| R14 | 18K ohms ± 2% Electrosyl TR5 | 403/4/78127/479 |
| R15 | 15038 ohms ± 0.1% MORGANITE FC55 | 620/4/06214 |
| R16 | 273200 ohms ± 0.1% MORGANITE FC55 | 620/4/06211 |
| R17,40,44,58 | 10K ohms ± 2% Electrosyl TR5 | 403/4/78127/473 |
| R18 | 390 ohms ± 2% Electrosyl TR5 | 403/4/78127/439 |
| R19 | 3.3K ohms ± 2% Electrosyl TR5 | 403/4/78127/461 |
| R20 | 200 ohms ± 2% Electrosyl TR5 | 403/4/78127/432 |
| R23,24,39,45,49,56,57 | 6.8K ohms ± 2% Electrosyl TR5 | 403/4/78127/469 |
| R25,26,48,53 | 510 ohms ± 2% Electrosyl TR5 | 403/4/78127/442 |
| R28,31 | 3.9K ohms ± 2% Electrosyl TR5 | 403/4/78127/463 |
| R36 | 270 ohms ± 2% ELECTROSYL TR5 | 403/4/78127/435 |
| R47 | 5.1K ohms ± 2% ELECTROSYL TR5 | 403/4/78127/466 |
| R50 | 10K ohms ± 0.5% WELWYN 4034C | 403/4/78526/176 |

COMPONENTS LIST

Title ...RAMP AND DISTORTION GENERATORS, BAUDS MONITOR (Cont.).....

Drawing No. ..620/1/06325..... Issue No. .15.(Sht.1).11.(Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| R51 | 16.9K ohms ± 0.5% WELWYN 4034C | 403/4/78526/225 |
| R52 | 8.2K ohms ± 2% Electrosyl TR8 | 403/4/78285/377 |
| TRANSISTORS | | |
| TR1 | 2N2217 | 417/4/98518 |
| TR2,3,5,9,10,14 | 2N2369A | 417/4/98291 |
| TR4 | E110 | 417/4/97057/000 |
| TR6,7,13 | BCY72 | 417/4/98267/003 |
| TR8,11,15 | BC108 | 417/4/98082/001 |
| TR12 | BFY51 | 417/4/98085 |

## COMPONENTS LIST

Title ....INTERFACE....

Drawing No. ....620/1/06329.... Issue No. ....6....

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1 | 0.1 F + 10% 400V<br>MULLARD 344 51104 | 400/4/98569/036 |
| C2, 3 | 0.22 F + 50<br>- 25% 6V | |
| | ERIE TRANSCAP 811 T/6V/0.22 | 400/4/98190/016 |
| C4,6,7 | 4700pF + 10% 500V<br>ERIE 811K 350081 | 400/4/98113/011 |
| C5 | 2200pF ± 5%<br>LEMCO MR2515 | 424/4/98053/014 |
| C8 | 1000pF + 20% 500V<br>ERIE 831K2600 | 400/4/98642/027 |
| DIODES | | |
| D1 | 1N4148 | 415/4/98393/000 |
| INTEGRATED CIRCUITS | | |
| IC1, 3, 7 | SN7402N | 446/4/98063/003 |
| IC2 | SN7472N | 446/4/98063/026 |
| IC4, 6, 9, 11, 12 | SN7400N | 446/4/98063/000 |
| IC5 | SN7440N | 446/4/98063/019 |
| IC8 | SN7404N | 446/4/98063/006 |
| IC10 | SN74132N | 446/4/98063/050 |
| RESISTORS | | |
| R1 | 15K ohms ± 2% Electrosyl TR5 | 403/4/78127/477 |
| R2 | 10K ohms ± 2% Electrosyl TR5 | 403/4/78127/473 |
| R3, 7, 9, 14 | 33K ohms ± 2% Electrosyl TR5 | 403/4/78127/485 |
| R4, 5, 6, 13, 20, 21,22 | 1K ohms ± 2% Electrosyl TR5 | 403/4/78127/449 |
| R8, R19 | 6.8K ohms ± 2% Electrosyl TR5 | 403/4/78127/469 |

## COMPONENTS LIST

Title ....INTERFACE (Cont'd).....

Drawing No. ....620/1/06329..... Issue No. 6.....

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| R10, 11, 12 & 23 | 330 ohms ± 2% Electrosyl TR5 | 403/4/78127/437 |
| R15, R16 | 4.7K ohms ± 2% Electrosyl TR5 | 403/4/78127/465 |
| R17 | 9.1K ohms ± 1% WELWYN 4034D | 403/4/78526/186 |
| R18 | 2.2K ohms ± 2% Electrosyl TR5 | 403/4/78127/457 |
| TRANSISTORS | | |
| TR1, 2, 3, 4. | MULLARD BC108 | 417/4/98082/001 |

COMPONENTS LIST

Title MESSAGE GENERATOR

Drawing No. 620/1/06343 Issue No. 7

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1, 2 | 0.1μF ± 20% 50V ERIE REDCAP 8131M | 447/4/98004/012 |
| C3 | 0.22μF ± 20% 50V ERIE REDCAP 8131M | 447/4/98004/016 |
| C4, C5 | 0.22μF 6V ERIE TRANSCAP 831/T/6V/0.22 | 400/4/98190/016 |
| DIODES | | |
| D1 | ZENER, MULLARD BZX70C10 | 415/4/98537/008 |
| D2 | TRANSITRON IN645 | 415/4/98034/017 |
| INTEGRATED CIRCUITS | | |
| IC15 | TEXAS TMS-2A - 41XX-MH | 620/4/06297 |
| IC1, 2, 3 | SN7406N | 446/4/98063/009 |
| IC4 | SN7470N | 446/4/98063/025 |
| IC5, 6, 7 | SN7474N | 446/4/98063/028 |
| IC8 | SN7430N | 446/4/98063/018 |
| IC9, IC10, IC12 | SN7400N | 446/4/98063/000 |
| IC11 | SN7402N | 446/4/98063/003 |
| IC14 | SN7420N | 446/4/98063/017 |
| IC13 | SN7404N | 446/4/98063/006 |
| RESISTORS | | |
| R1,4,7,10,24 to 33 | 2.2K ohms ± 2% Electrosyl TR5 | 403/4/78127/457 |
| R2,3,5,6,8,9,11 to 23 | 10K ohms ± 2% Electrosyl TR5 | 403/4/78127/473 |
| R34 | 680 ohms ± 2% Electrosyl TR5 | 403/4/78127/445 |
| R35 - 45, 49 | 1K ohms ± 2% Electrosyl TR5 | 403/4/78127/449 |
| R46, R47 | 4.7K ± 2% Electrosyl TR5 | 403/4/78127/465 |
| R48 | 220Ω ± 2% Electrosyl TR5 | 403/4/78127/433 |
| R50 | 470Ω ± 2% Electrosyl TR5 | 403/4/78127/441 |
| TRANSISTORS | | |
| TR1 to 7 | MULLARD BC108 | 417/4/98082/001 |
| TR8 | MULLARD BFY51 | 417/4/98085 |

## COMPONENTS LIST

Title ..... OPTIONAL MESSAGE GENERATOR .....

Drawing No. ..... 620/1/06889/000 ..... Issue ..... 3 .....

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1-3 | 0.047μF, 12V, ERIE | 400/4/98710/004 |
| DIODES | | |
| D1 | Transitron IN645 | 415/4/98034/017 |
| INTEGRATED CIRCUITS | | |
| IC1, 5, 10 | SN7400N | 446/4/98063/000 |
| IC2, 4 | SN7493AN | 446/4/01198/002 |
| IC3 | IM5603 | 620/7/06890/000 |
| IC6 | SN7404N | 446/4/98063/006 |
| IC7 | SN7432N | 446/4/98063/038 |
| IC8 | IM5603 | 620/7/06890/001 |
| IC9 | SN7410N | 446/4/98063/013 |
| IC11 | SN7406N | 446/4/98063/009 |
| RESISTORS | | |
| R1-15, R20-25 | 1K ± 2% Electrosyl TR5 | 403/4/78127/449 |
| R16 | 220 ± 2% Electrosyl TR5 | 403/4/78127/433 |
| R17 | 470 ± 2% Electrosyl TR5 | 403/4/78127/441 |
| R18, R19 | 4.7K ± 2% Electrosyl TR5 | 403/4/78127/465 |
| TRANSISTORS | | |
| TR1 | BFY51 | 417/4/98085 |

## COMPONENTS LIST

Title ...SERIALISER.....

Drawing No. ..620/1/06331..... Issue No. ... ...6.....

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1, 3 | 0.22μF + 50% - 25% 6V ERIE 811/T/6V | 400/4/98190/016 |
| C2 | 10,000pF ± 25% 300V ERIE 811 K7004 | 400/4/98376/009 |
| DIODES | | |
| D1, 2 | IN 4148 | 415/4/98393 |
| INTEGRATED CIRCUITS | | |
| IC1, 4, 11, 13, 15, 19 | SN7400N | 446/4/98063/000 |
| IC2 | SN7430N | 446/4/98063/018 |
| IC3, 6, 9, 10, 12 | SN7420N | 446/4/98063/017 |
| IC5, 14, 18 | SN7470N | 446/4/98063/025 |
| IC7, 16 | SN7410N | 446/4/98063/013 |
| IC8, 17 | SN7474N | 446/4/98063/028 |
| RESISTORS | | |
| R1, 2, 9 to 18 | 1K ohm ± 2% Electrosyl TR5 | 403/4/78127/449 |
| R3 | 2.2K ohm ± 2% Electrosyl TR5 | 403/4/78127/457 |
| R4 | 510 ohms ± 2% Electrosyl TR5 | 403/4/78127/442 |
| R5 | 1.8K ohms ± 2% Electrosyl TR5 | 403/4/78127/455 |
| R6 | 10K ohms ± 2% Electrosyl TR5 | 403/4/78127/473 |
| R7, 8 | 6.8K ohms ± 2% Electrosyl TR5 | 403/4/78127/469 |
| R19 | 8.2K ohms ± 2% ELECTROSYL TR8 | 403/4/78285/377 |
| TRANSISTORS | | |
| TR1 | MULLARD BCY72 | 417/4/98267/003 |
| TR2 | MULLARD BC108 | 417/4/98082/001 |

## COMPONENTS LIST

Title ...ELECTRONIC OUTPUT.....

Drawing No. ..620/1/1/06327..... Issue No. 8 (Sht.1) A (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| CAPACITORS | | |
| C1 | 0.022μF + 50% - 25% 18V<br>ERIE TRANSCAP 831/T/18V | 400/4/98190/054 |
| C2, 3 | 0.22μF + 50% - 25% 6V<br>ERIE TRANSCAP 811/T/6V | 400/4/98190/016 |
| C4, 5 | 150pF ± 10%<br>ERIE SN1300YD TUBULAR CERAMIC | 400/4/98595/060 |
| C6, 7. | 2200pF ± 10%<br>ERIE 811 K 170051 | 400/4/98112/012 |
| C8, 9. | 0.15μF 100V<br>MULLARD 344 25154 | 400/4/98785/004 |
| COILS | | |
| L1, 3 | 33mH CAMBION 3635-55 | 406/4/98002/055 |
| L2, 4 | 470μH PAINTON 58/10/0021/10 | 406/4/98012/012 |
| DIODES | | |
| D1, 2, 3, 6, 7 | IS920 | 415/4/98153/001 |
| D4,5,8,9,10,11,12,13 | HS9099 | 415/4/98316/008 |
| D14, 15 | LUCAS DA002 (SPECIAL) | 415/4/98216/005 |
| RESISTORS | | |
| R1, 2, 14, 15, 23, 26 | 680 ohms ± 2% ELECTROSYL TR5 | 403/4/78127/445 |
| R3 | 2.2K ohms ± 2% Electrosyl TR5 | 403/4/78127/457 |
| R4, 5, 8 | 1.5K ohms ± 2% Electrosyl TR5 | 403/4/78127/453 |
| R6, 7, 11, 16 | 3.9K ohms ± 2% Electrosyl TR5 | 403/4/78127/463 |
| R9, 10 | 1.2K ohms ± 2% Electrosyl TR5 | 403/4/78127/451 |
| R12, 17, 22, 25 | 1K ohms ± 2% Electrosyl TR5 | 403/4/78127/449 |

## COMPONENTS LIST

Title ...ELECTRONIC OUTPUT.....

Drawing No. ..620/1/06327..... Issue No. 8 (Sht.1) 4 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| RESISTORS (Continued) | | |
| R13 | 1.8K ± 2% Electrosyl TR5 | 403/4/78127/455 |
| R18, 19 | 5.6K ± 2% Electrosyl TR5 | 403/4/78127/467 |
| R20, 21 | 10K ohms ± 2% ELECTROSYL TR5 | 403/4/78127/473 |
| R24, 27 | 180 ohms ± 2% Electrosyl TR5 | 403/4/78127/431 |
| R28, 30 | 820 ohms ± 2% Electrosyl TR5 | 403/4/78127/447 |
| R29, 31 | 270 ohms ± 2% Electrosyl TR5 | 403/4/78127/435 |
| R32, 38 | 150 ohms ± 2% Electrosyl TR5 | 403/4/78127/429 |
| R33, 39 | 82 ohms ± 2% Electrosyl TR5 | 403/4/78127/423 |
| R34, 40 | 39 ohms ± 2% Electrosyl TR5 | 403/4/78127/415 |
| R35, 41 | 20 ohms ± 2% Electrosyl TR5 | 403/4/78127/408 |
| R36, 42 | 2.7 ohms CGS C3A | 403/4/78355/030 |
| R37, 43 | 10 ohms CGS C3A | 403/4/78355/037 |
| TRANSFORMERS | | |
| T1, 2 | | 620/1/06341 |
| TRANSISTORS | | |
| TR1 to 8, 11, 16 to 19 | 2N2369A | 417/4/98291 |
| TR9,10,12,13,21,24 | BCY72 | 417/4/98267/003 |
| TR14, 15 | 2N3576 | 417/4/ 05116 |
| TR20, 23 | 2N3739 | 417/4/98273/002 |
| TR22, 25 | BC108 | 417/4/98082/001 |

## COMPONENTS LIST

**Title** .FRONT PANEL ASSEMBLY.....

**Drawing No.** ...620/1/07095..... **Issue No.** .1 (Sht.1) 1 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| Refer to Fig. 8.6 | | |
| LAMPS & LED | | |
| ILP1 | Lamp Neon 110V | 517/4/98105/001 |
| ILP2 | LED Hewlett Packard 5082-4440 | 517/4/98129/001 |
| POTENTIOMETERS | | |
| R1 | 5K ohms ± 10% 3 turn Helipot | 404/4/05035 |
| R2 | 1K ohms ± 10% 5 turn Helipot | 404/4/05036 |
| SWITCHES | | |
| S1 | Stop Element (2 - pole, 8 - way) | 620/4/06335 |
| S2-S8, S14 | Keys and Mains on/off (Arrow Type 110022E) | 408/4/50416/000 |
| S9 | Parity (Rocker Switch, Arrow Type 110021E) | 408/4/50416/002 |
| S10, S18 | Test Message and Signal (1 - pole, 4 - way) | 620/4/06336 |
| S11 | Run/Stop (Rocker Switch, Arrow Type 110223E) | 408/4/50416/001 |
| S12 | Step Pushbutton (Render Instr. Type PB5 - 1 - C.O.) | 408/4/98274/002 |
| S13 | Speed Selector | 620/1/06241 |
| S15 | Distortion (8 - pole, 5 - way) | 620/4/06337 |
| S16 | Mark Polarity (Carlingswitch T1LB60/5C/WH/A) | 408/4/98357/007 |
| S17 | Supply (4-pole, 4-way) | 620/4/07094 |

## COMPONENTS LIST

Title REAR PANEL ASSEMBLY

Drawing No. 620/1/06860 Issue No. 1 (Sht.1) 1 (Sht.2)

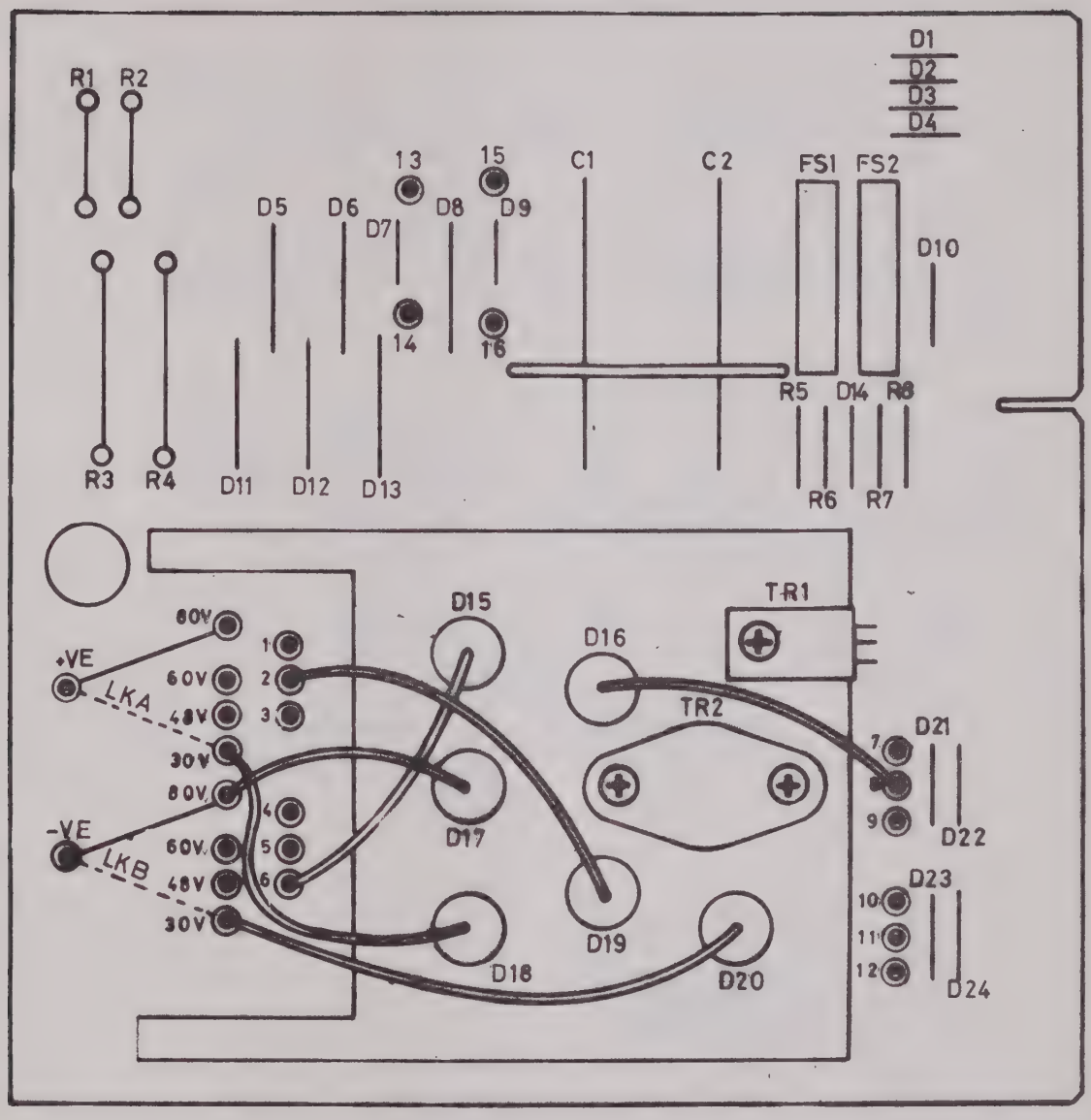
| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| Refer to Fig.8.6 | | |
| Fuses | | |
| FS1 | 250mA Slow Blow 20mm x 5mm | 518/4/98037/005 |
| FS2 | 500mA Slow Blow 20mm x 5mm | 518/4/98037/008 |
| FS3,4 | 250mA Quick Blow 20mm x 5 mm | 518/4/98052/018 |
| Sockets | Socket 15-way Canon DA155 | 508/4/28179/005 |
| Voltage Selector | | 620/1/06658 |

## COMPONENTS LIST

Title ..... CHASSIS ASSEMBLY .....

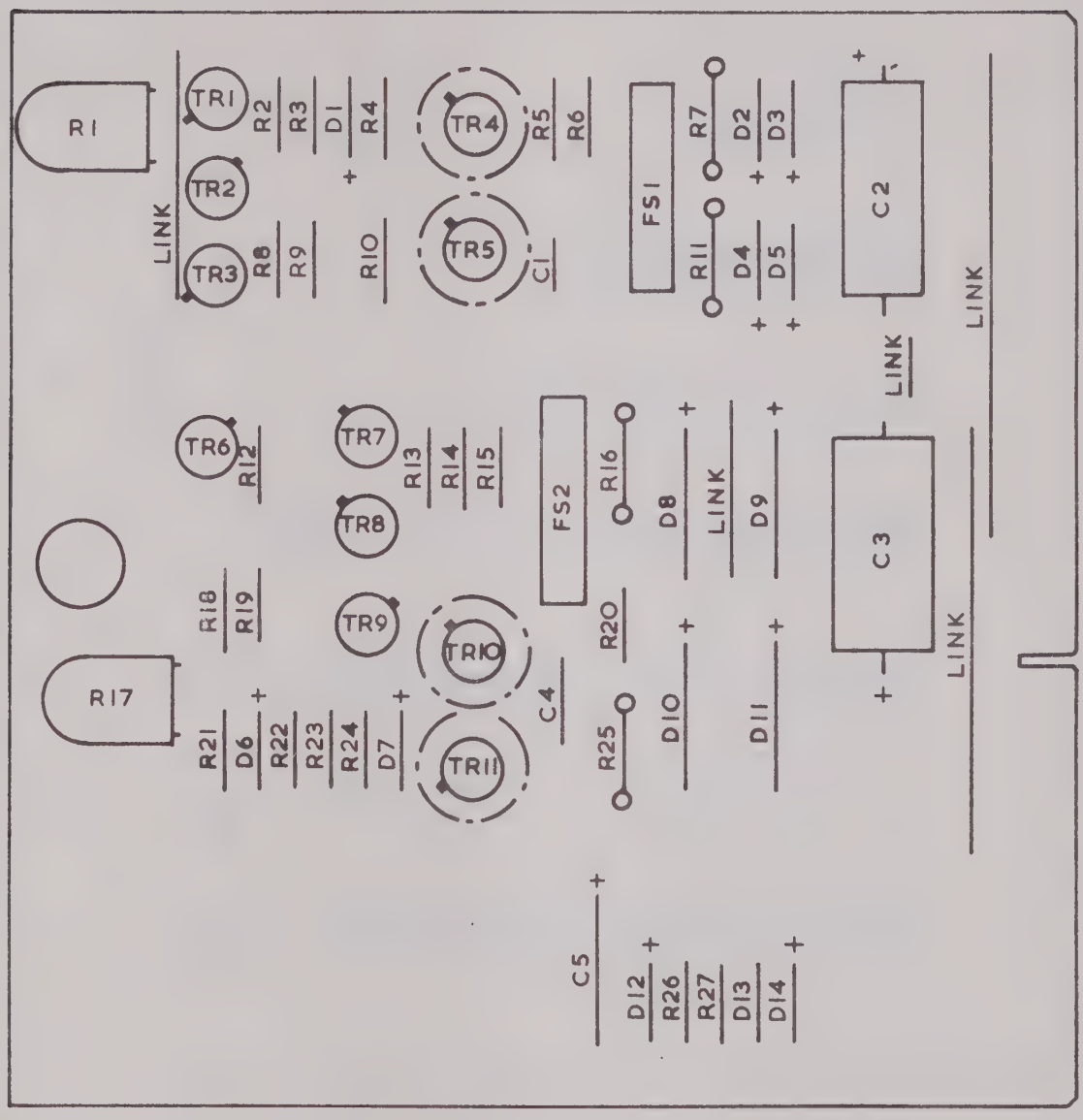
Drawing No. ..... 620/1/06322 ..... Issue No. 11 (Sht.1) 8 (Sht.2)

| Circuit Reference | Description | Plessey Part No. |
|---|---|---|
| Refer to Fig. 8.6 | | |
| CAPACITORS | | |
| C1 | 1500µF 63V Electrolytic<br>MULLARD 071/18152 | 402/4/98194/021 |
| C2 | 10000µF 16V Electrolytic<br>MULLARD 071/15103 | 402/4/98194/010 |
| INTERFERENCE SUPPRESSOR | | |
| FL1 | | 412/8/01021/002 |
| TRANSFORMER | | |
| T1 | | 620/4/06338 |
| TRANSISTOR | | |
| TR1, 2 | BDY92<br>MULLARD | 417/4/98721/002 |
| THYRISTOR | BTY 79 100R MULLARD | 415/4/98258/002 |



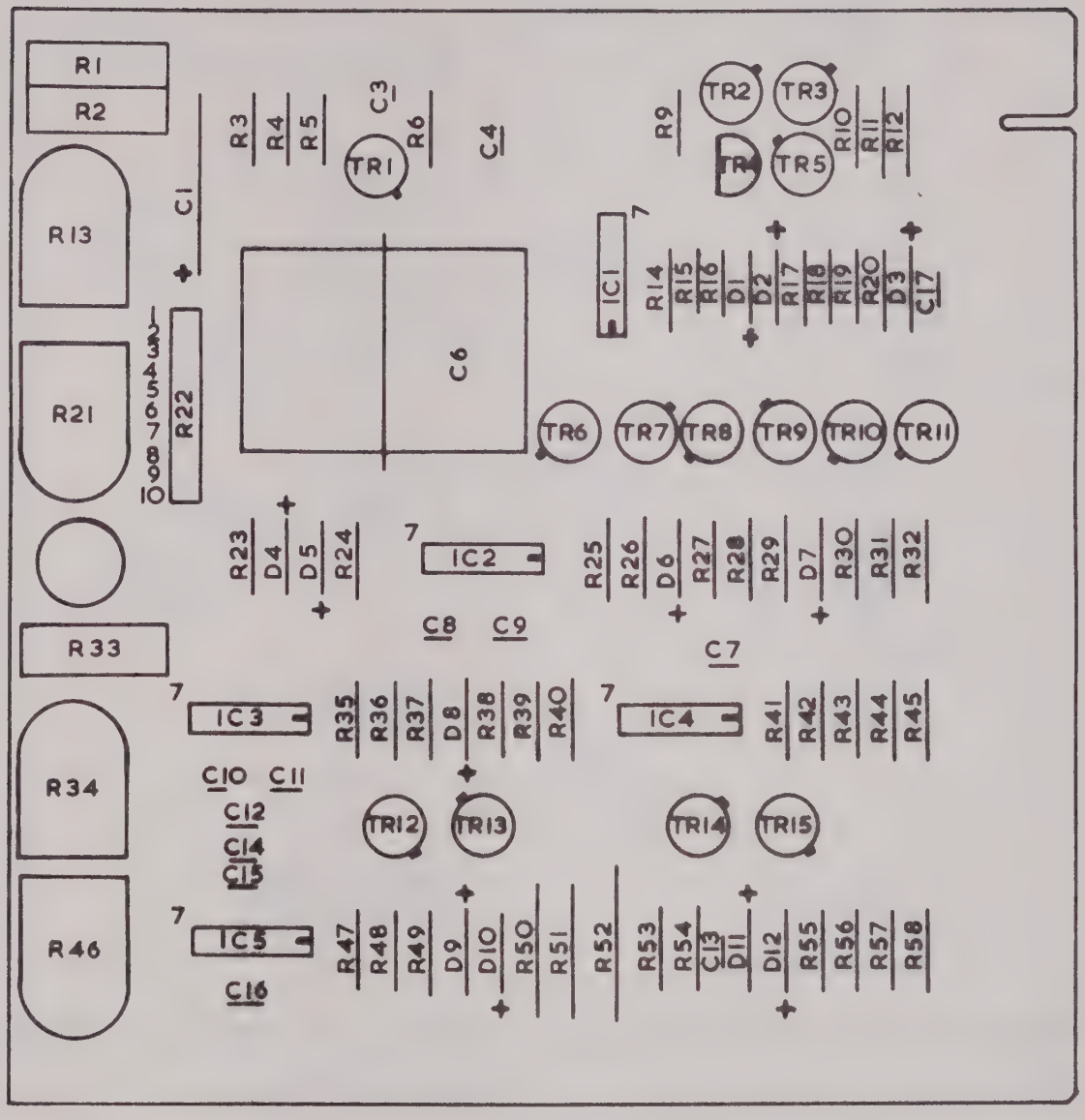

620/1/07097/000 Iss. 1

Figure 7.1 Telegraph Battery Board Layout



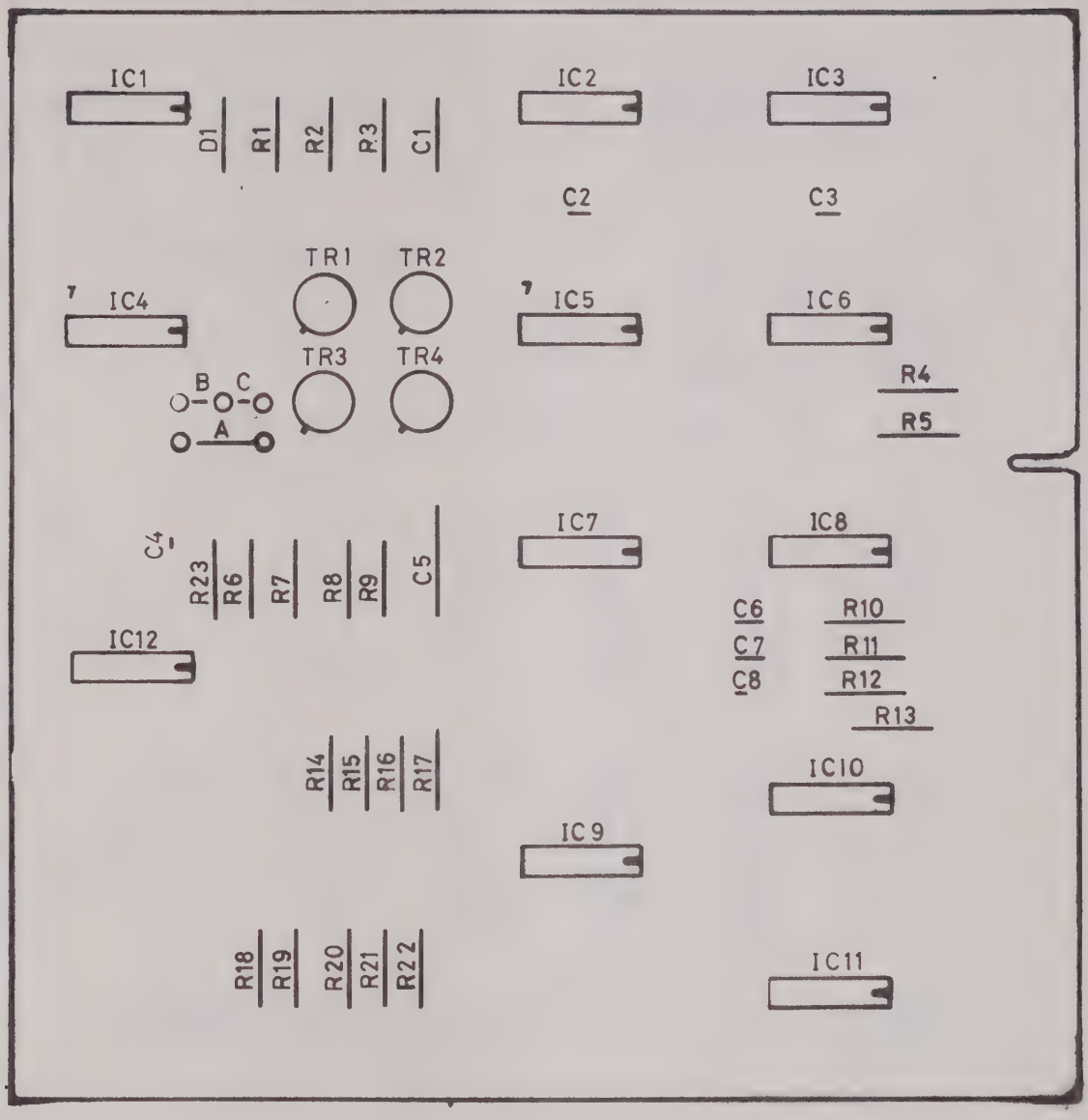

620/1/06347 Iss. 3

Figure 7.2 Power Supply Board Layout



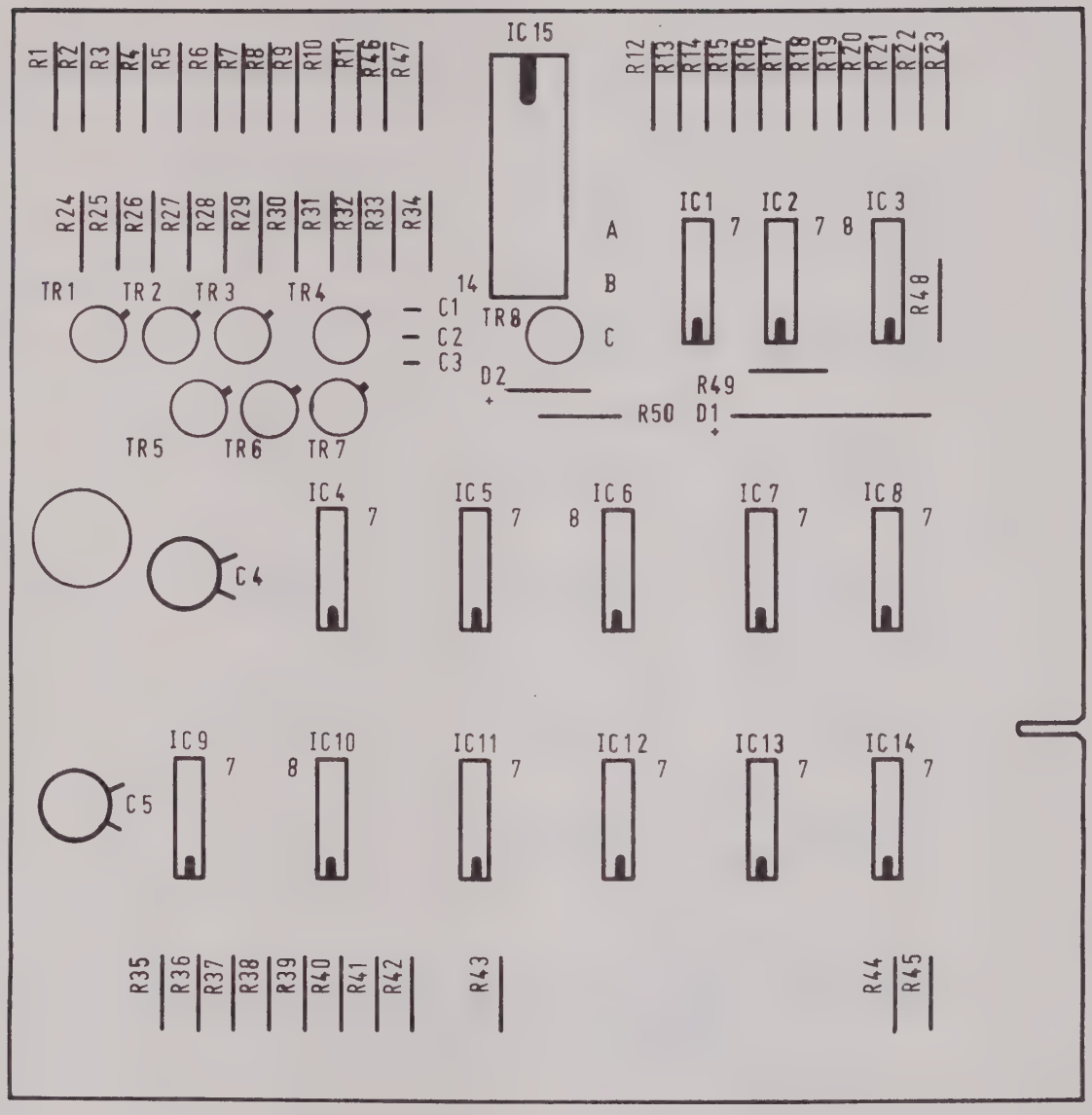

620/1/06325 Iss. 5

Figure 7.3 Ramp and Distortion Board Layout



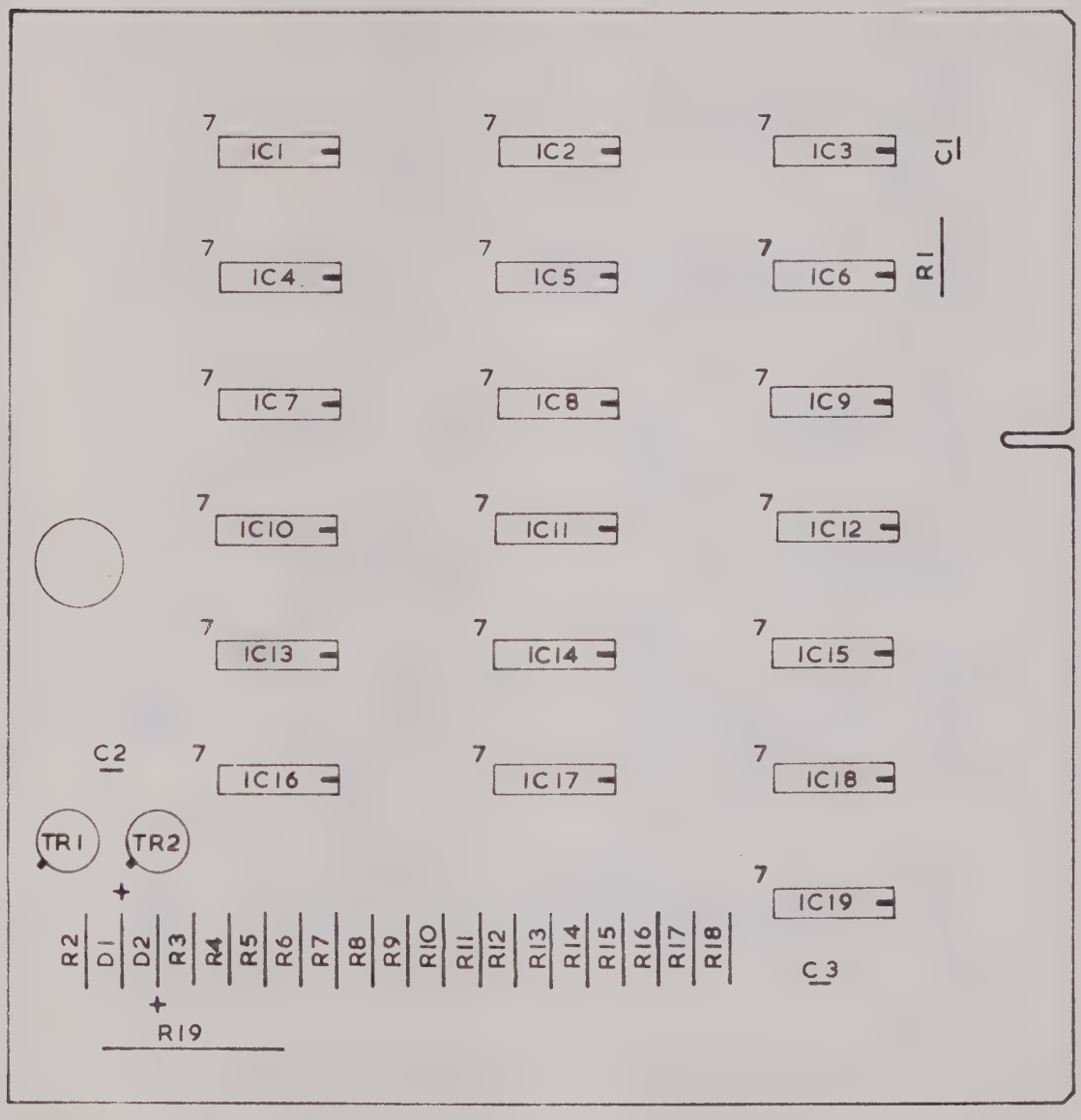

620/1/06329 Iss. 4

Figure 7.4 Interface Board Layout



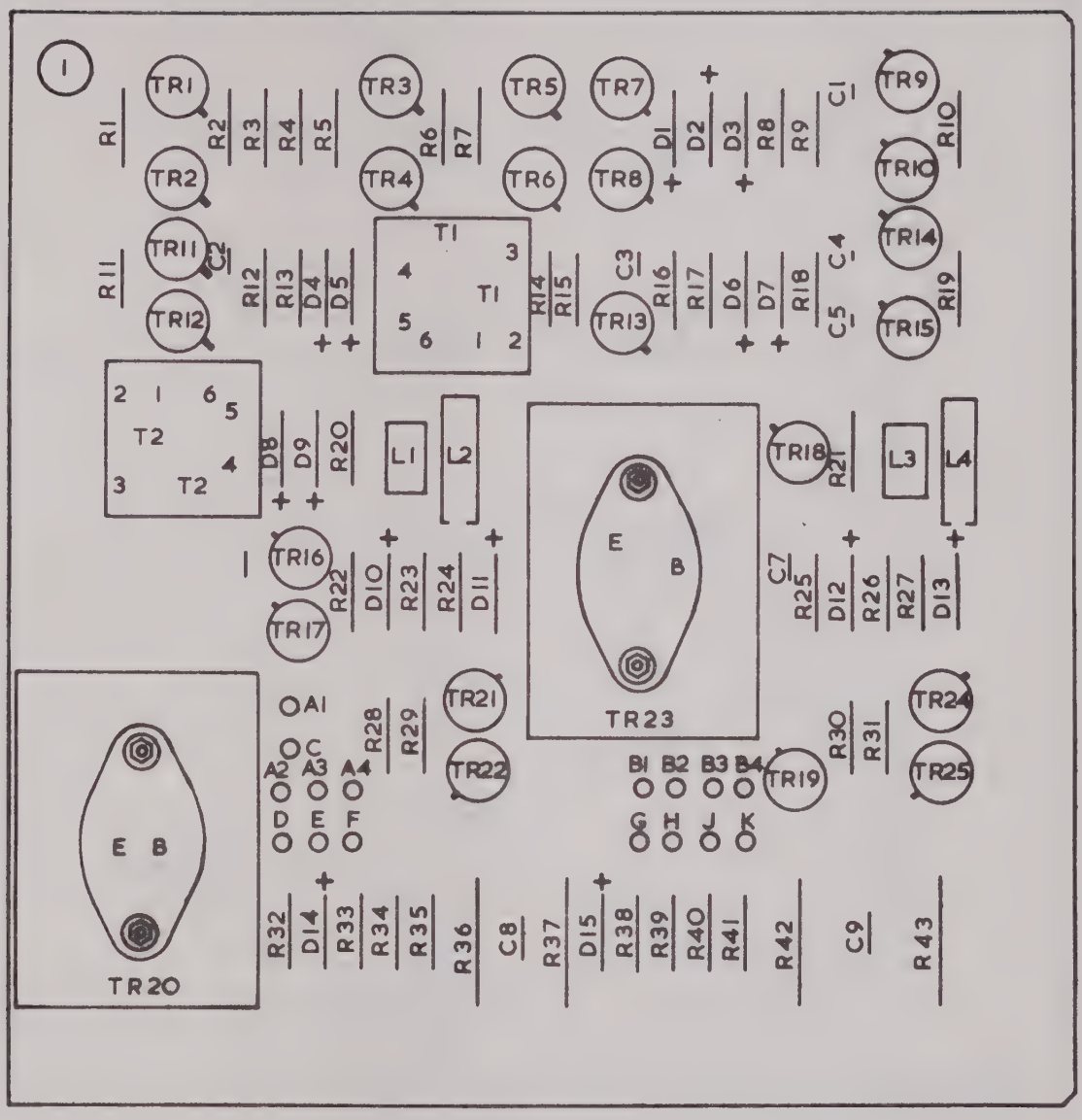

620/1/06343/ETC. Iss. 5

Figure 7.5 Message Generator Board Layout



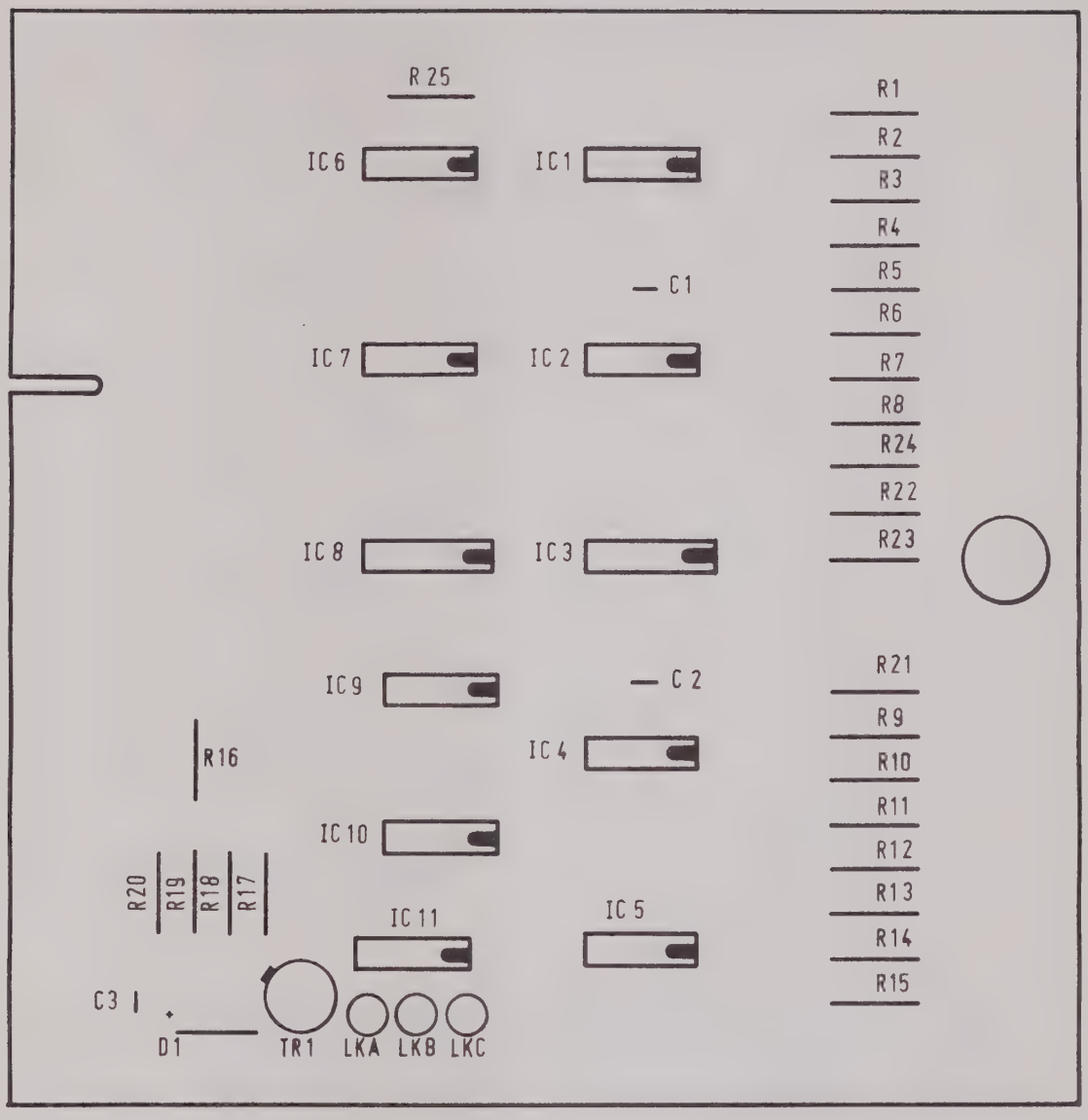

620/1/06331 Iss. 1

Figure 7.6 Serialiser Board Layout




620/1/06327 Iss. 5

Figure 7.7 Electronic Output Board Layout




620/1/06889/ETC. Iss. 3

Figure 7.8 Optional Message Generator Board Layout

End of Section 7

# TELEGRAPH SIGNAL GENERATOR

## TSG 40.2

## SECTION 8 - DIAGRAMS

## CONTENTS

8.1 FRONT PANEL

8.2 REAR VIEW

8.3 TOP VIEW - COVER REMOVED

8.4 TEST MESSAGES

8.5 5 UNIT CODE

8.6 CIRCUIT DIAGRAM

8.7 TELEGRAPH BATTERY

8.8 POWER SUPPLY

8.9 RAMP GENERATOR

8.10 INTERFACE

8.11 INTERFACE WAVEFORMS

8.12 MESSAGE GENERATOR

8.13 SERIALISER

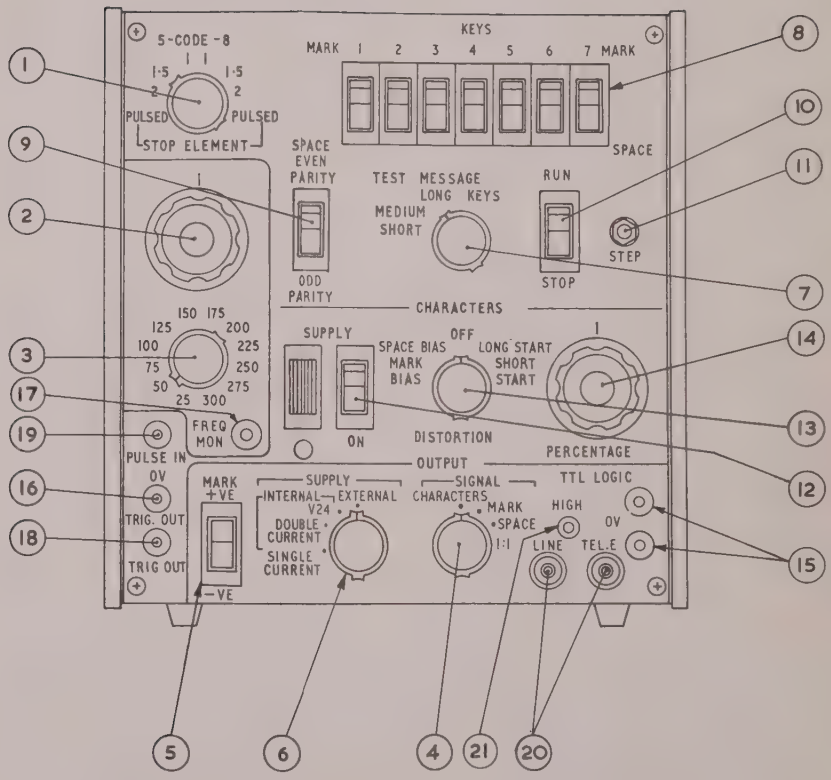
8.14 SERIALISER COUNTER AND MULTIPLEXER WAVEFORMS (8 Level)

8.15 SERIALISER COUNTER AND MULTIPLEXER WAVEFORMS (5 Level)

8.16 SERIALISER DATA CONTROLLER AND OUTPUT WAVEFORMS

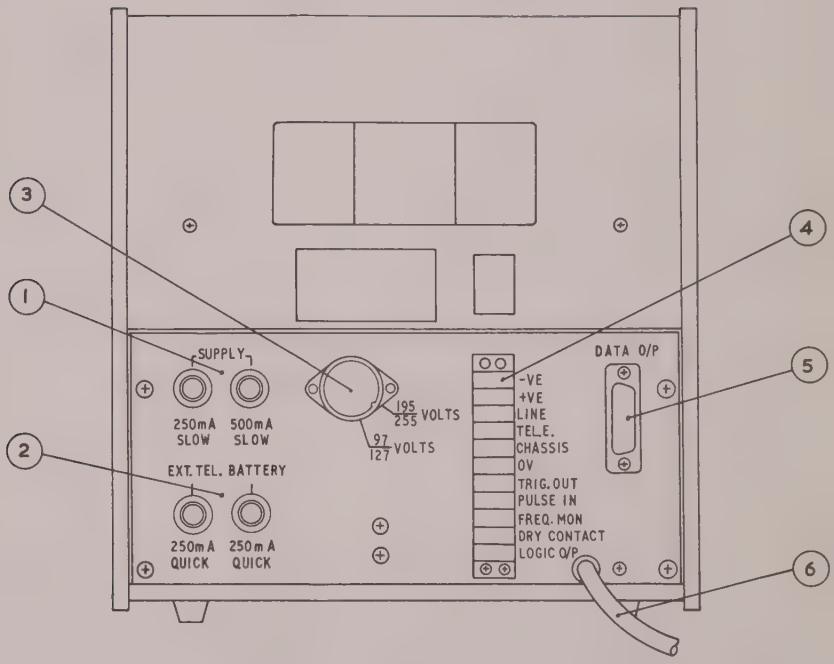
8.17 ELECTRONIC OUTPUT

8.18 OPTIONAL MESSAGE GENERATOR



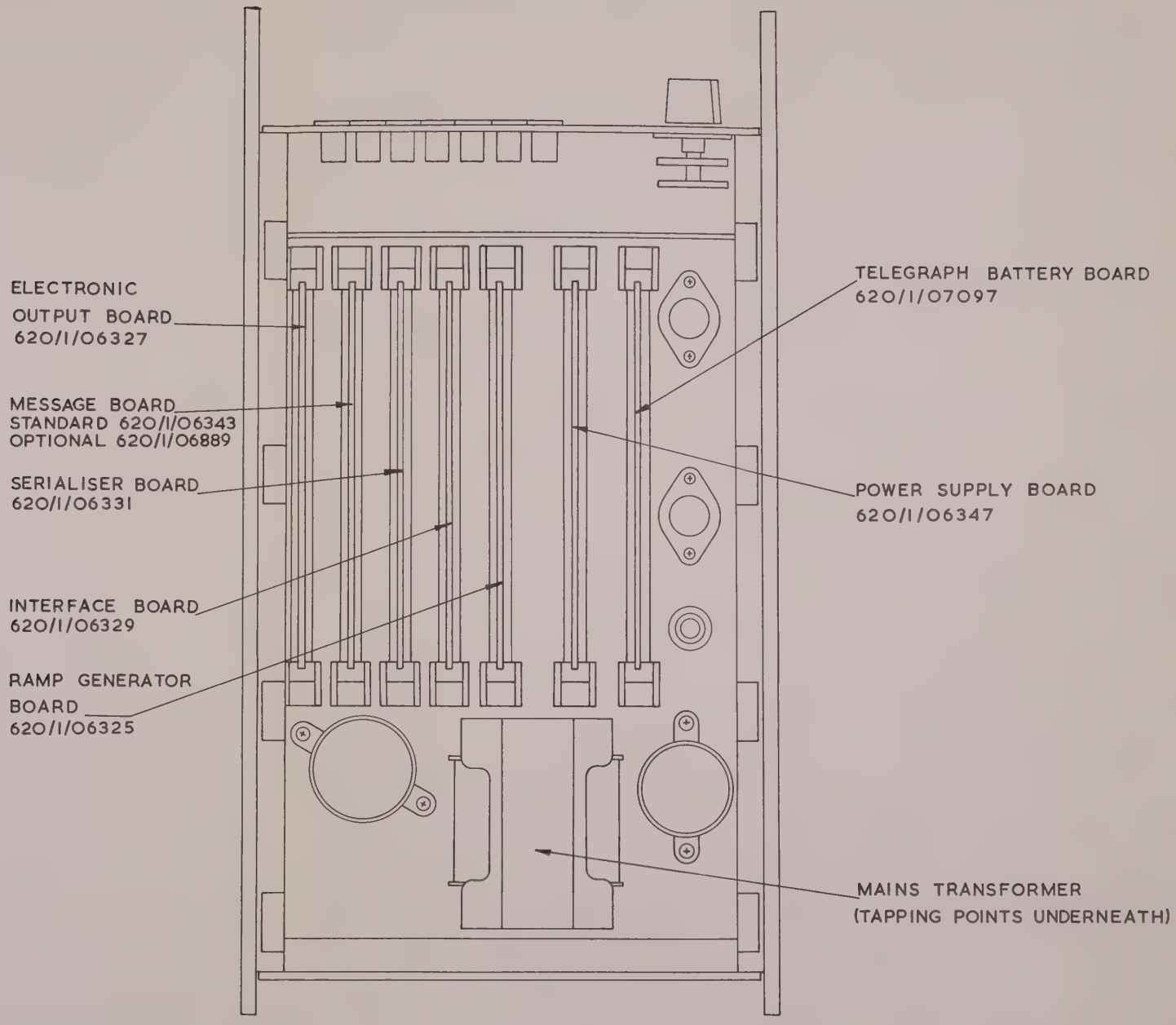

FRONT PANEL FIG. 8.1

620/8/06320/002 SHT.1 ISS.1.




REAR VIEW

FIG. 8.2




TOP VIEW - COVER REMOVED

FIG. 8.3

## C.C.I.T.T. NO.5 (8 UNIT)

LONG TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | < | ≡ | T | · | · | e | < | > | > | s | < | > | > | > | T | > | T | h | E | > | Q | u | i | c |

| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | K | > | B | r | o | w | N | > | F | o | X | > | j | u | m | p | S | > | 0 | v | e | R | > | T |

| CHARACTER NO. | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | h | E | > | L | a | z | Y | > | D | o | G | > | 1 | 2 | 3 | , | 4 | 5 | 6 | 7 | > | 8 | 9 | ø |

| CHARACTER NO. | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | > | : | · | ? | > | - | = | + | + | + | + | + | ' | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL |

MEDIUM TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | < | ≡ | T | E | S | T | > | > | U | * | U | * | U | * | U | * | U | * | U | * | U | * | U | * |

| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
|---|---|---|---|---|---|---|---|---|
| TEXT | U | * | U | * | U | * | U | * |

SHORT TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| TEXT | DEL | S | < | ≡ | Q | DEL | > | 9 |

## C.C.I.T.T. NO. 2 (5 UNIT)

LONG TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | < | ≡ | T | < | > | E | < | > | > | S | < | > | > | > | T | ↑ | > | ↓ | T | H | E | > | Q |

| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | U | I | C | K | > | B | R | O | W | N | > | F | O | X | > | J | U | M | P | S | > | O | V | E |

| CHARACTER NO. | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | R | > | T | H | E | > | L | A | Z | Y | > | D | O | G | > | ↑ | 1 | 2 | 3 | > | 4 | 5 | 6 | 7 |

| CHARACTER NO. | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | > | 8 | 9 | ø | > | : | . | ? | > | - | = | + | + | + | + | + | + | + | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |

MEDIUM TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | < | ≡ | T | E | S | T | > | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y |

| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
|---|---|---|---|---|---|---|---|---|
| TEXT | R | Y | R | Y | R | Y | R | Y |

SHORT TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | S | < | ≡ | Q | ↑ | > | 9 |

LEGEND

< = CARRIAGE RETURN
≡ = LINE FEED
> = SPACE
DEL = DELETE
↓ = SHIFT TO LETTERS
↑ = SHIFT TO FIGURES

620/DJ/06320 SH 18 ISS 3

TEST MESSAGES TRANSMITTED BY TSG40

FIG. 8.4

## C.C.I.T.T. NO.5 (8 UNIT)

### LONG TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | | | T | < | | e | | | > | s | < | > | > | > | T | > | T | h | E | ? | Q | u | ı | c |
| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| TEXT | K | > | B | r | o | w | N | . | F | o | X | > | j | u | m | p | S | > | 0 | v | e | R | > | T |
| CHARACTER NO. | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 |
| TEXT | h | E | > | L | a | z | Y | | D | o | G | > | 1 | 2 | 3 | > | 4 | 5 | 6 | 7 | : | 8 | 9 | ø |
| CHARACTER NO. | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 |
| TEXT | > | : | . | ? | > | - | - | + | + | + | + | + | + | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL | DEL |

### MEDIUM TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | < | = | T | E | S | T | ` | , | U | * | U | * | U | * | U | * | U | * | U | ▒ | U | ▒ | U | * |
| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | | | | | | | | | | | | | | | | |
| TEXT | U | * | U | + | U | * | U | * | | | | | | | | | | | | | | | | |

### SHORT TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| TEXT | DEL | S | < | = | Q | DEL | , | 9 |

## C.C.I.T.T. NO. 2 (5 UNIT)

### LONG TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | < | - | T | < | > | E | , | > | > | S | < | > | > | > | T | ↑ | ` | ↓ | T | H | E | > | Q |
| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| TEXT | U | I | C | K | > | B | ▒ | 0 | W | N | > | F | 0 | X | > | J | U | M | P | S | > | 0 | V | E |
| CHARACTER NO. | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 |
| TEXT | R | > | T | H | E | > | L | A | Z | Y | > | D | 0 | G | > | ↑ | 1 | 2 | 3 | > | 4 | 5 | 6 | 7 |
| CHARACTER NO. | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 |
| TEXT | > | 8 | 9 | ø | > | : | . | ? | > | - | = | + | + | + | + | + | + | + | ` | ↓ | ↓ | ↓ | ↓ | ↓ |

### MEDIUM TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | < | = | T | E | S | T | > | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y | R | Y |
| CHARACTER NO. | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | | | | | | | | | | | | | | | | |
| TEXT | R | Y | R | Y | R | Y | R | Y | | | | | | | | | | | | | | | | |

### SHORT TEST MESSAGE

| CHARACTER NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| TEXT | ↓ | S | < | = | Q | ↑ | > | 9 |

LEGEND

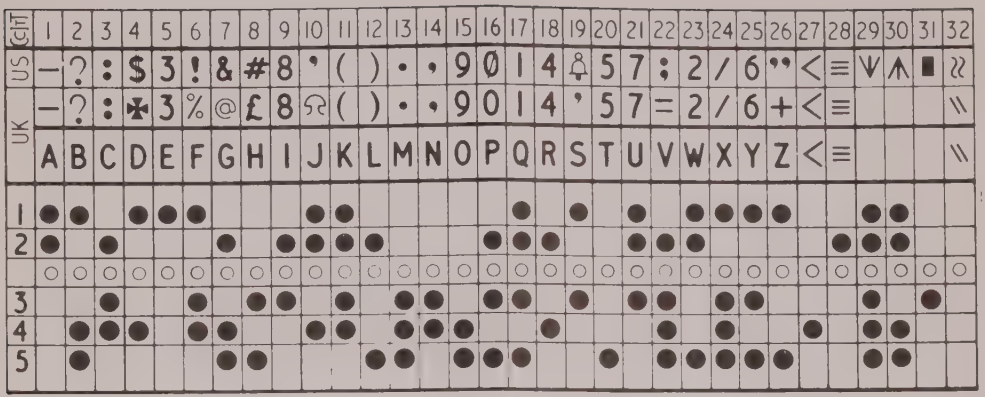
< = CARRIAGE RETURN
= = LINE FEED
> = SPACE
DEL = DELETE
↓ = SHIFT TO LETTERS
↑ = SHIFT TO FIGURES

TEST MESSAGES TRANSMITTED BY TSG40

FIG. 8.4

620/DJ/06320 SH 18 ISS 3

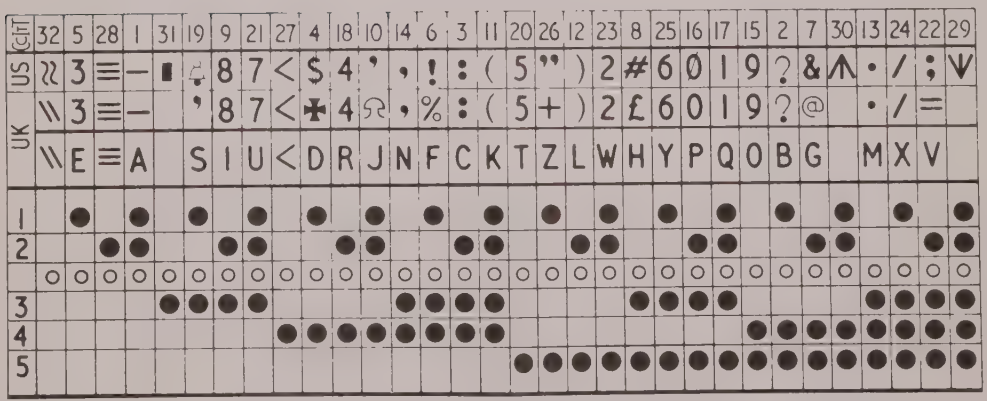
656/MA/00990/100 Sheet 1




(a)

5 Unit Code Key settings in alphabetical order

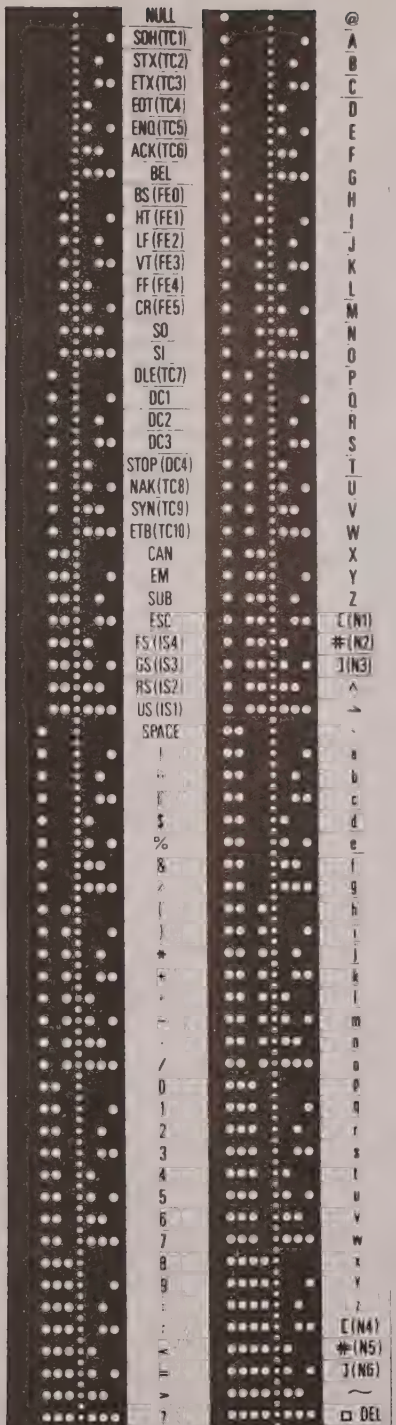
656/MA/00990/199 Sheet 2




(b)

5 Unit Code Key settings in binary order

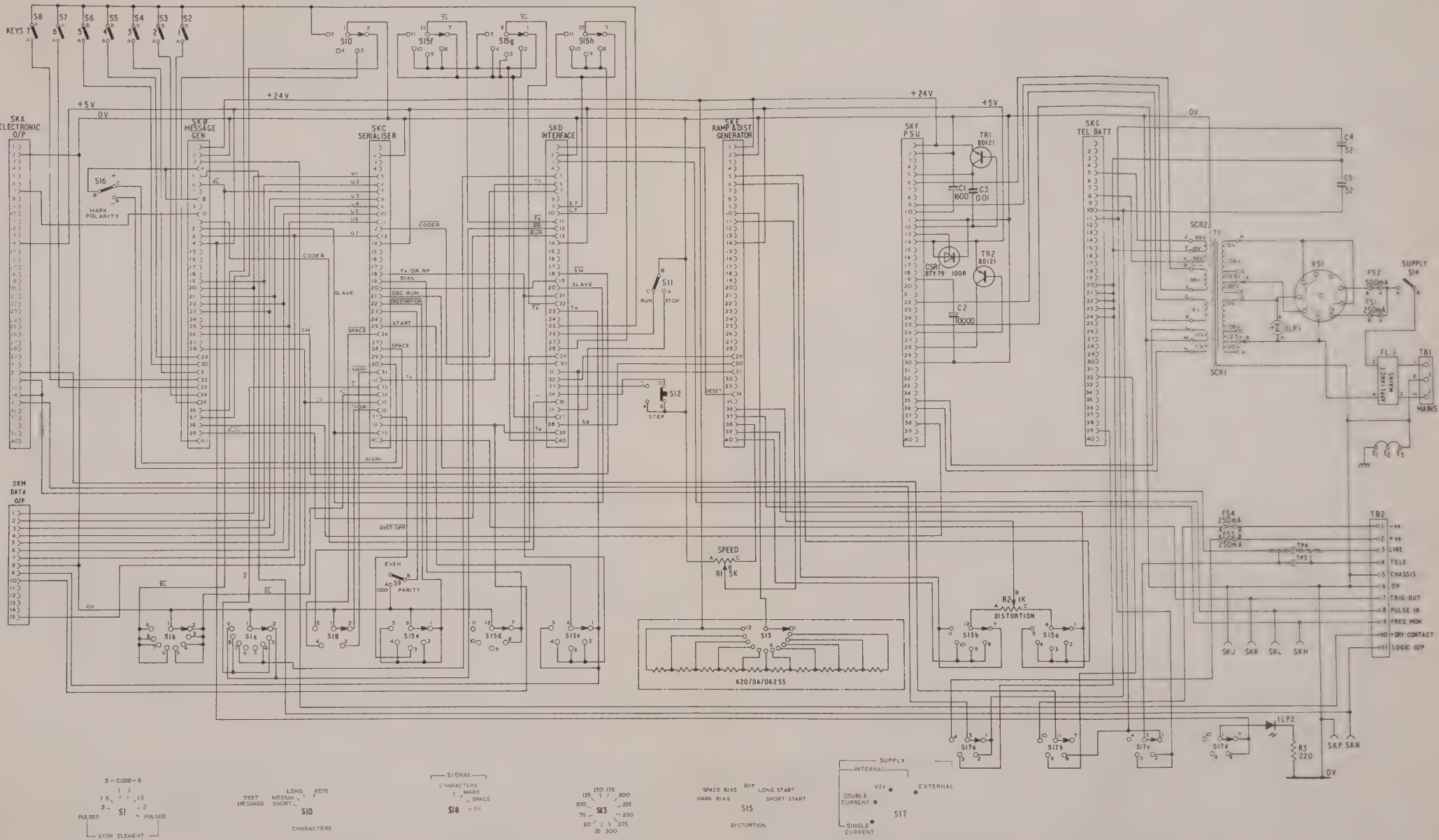
Fig 8.5
Sheet 1




(c)

8 Unit Code Key settings

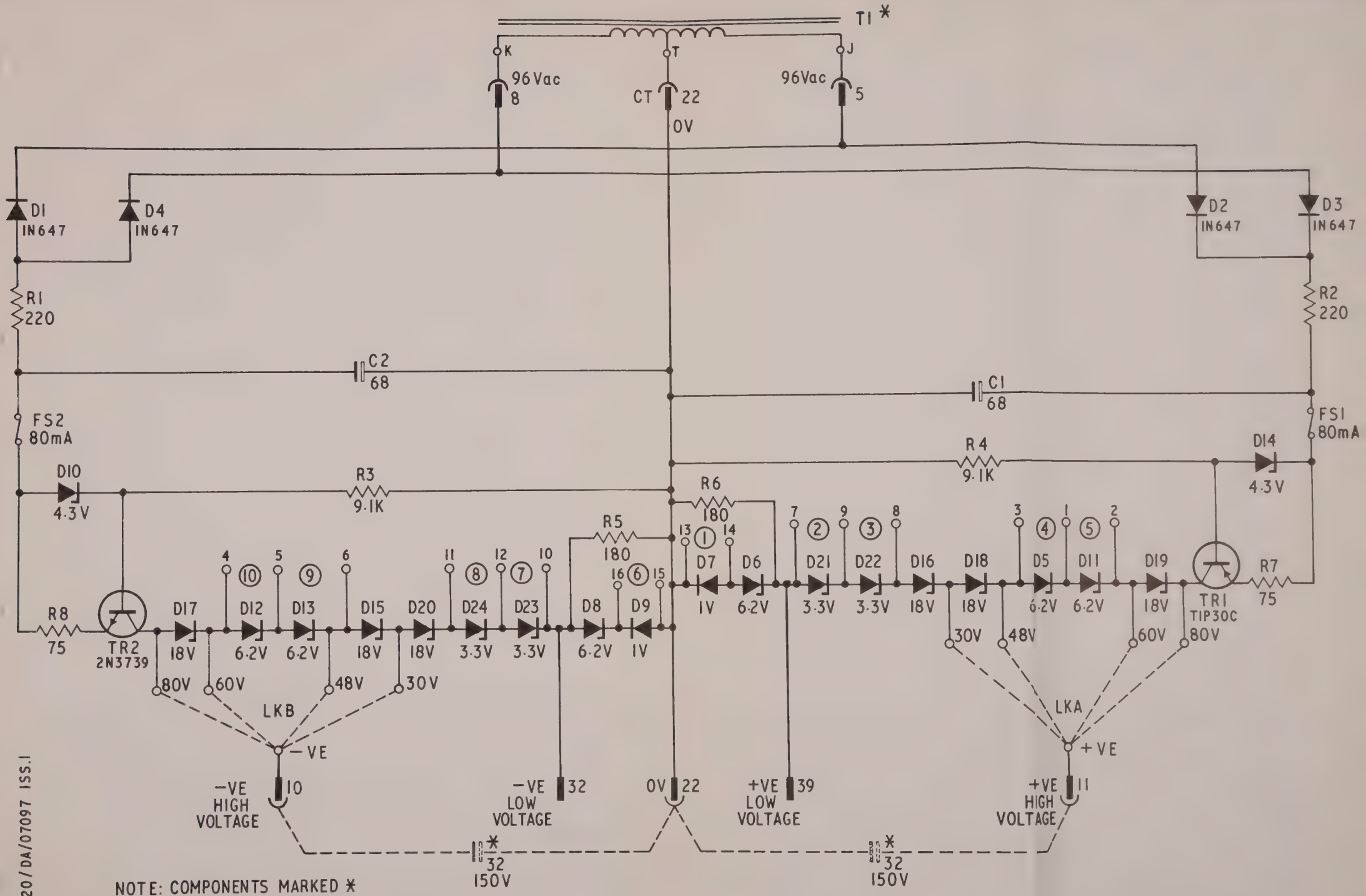
Fig. 8.5
Sheet 2




# TELEGRAPH SIGNAL GENERATOR

FIG. 8.6
TSG.40.2

620/DA/06320/002 ISS 3

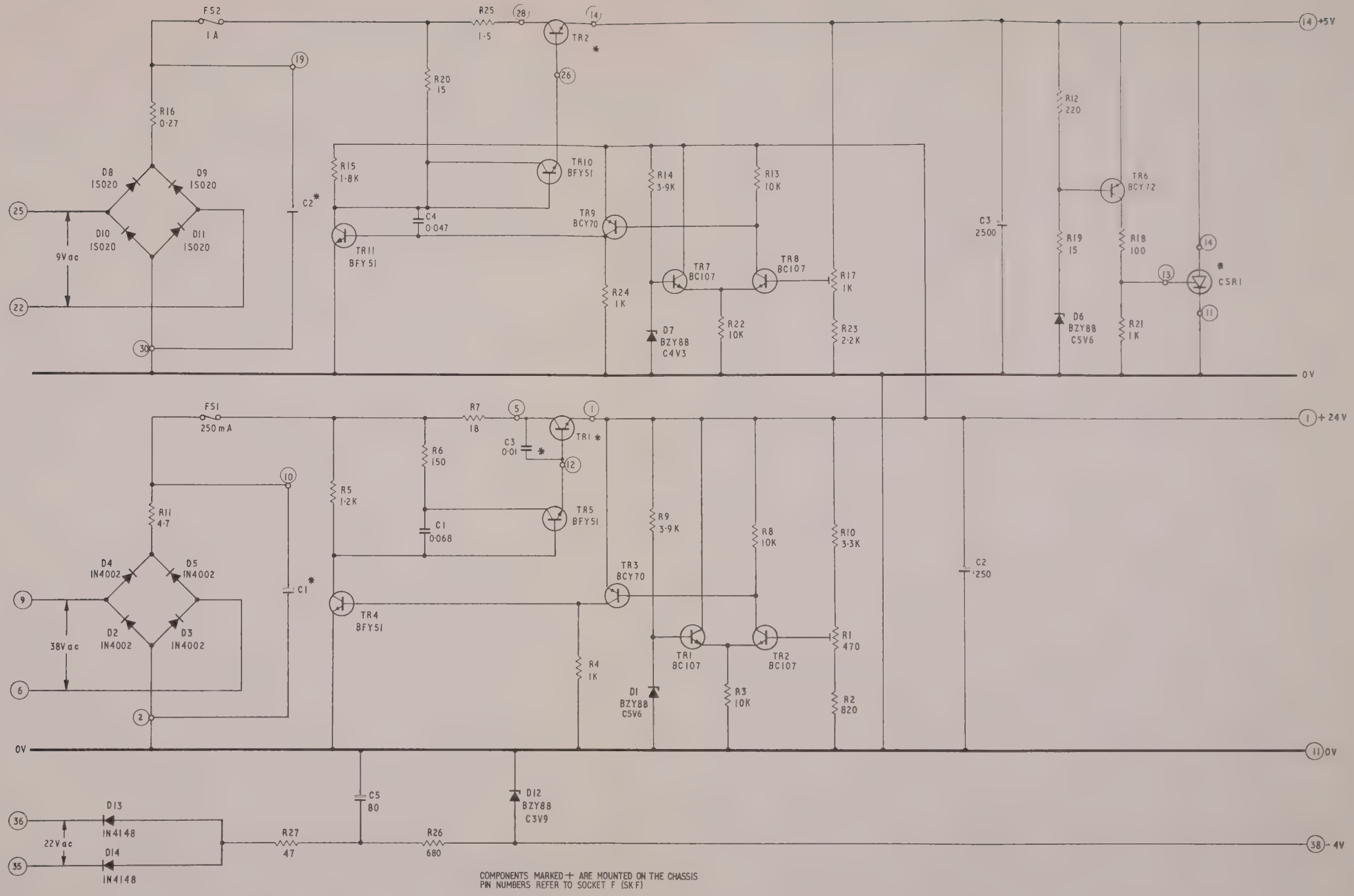



620/DA/07097 ISS.1

NOTE: COMPONENTS MARKED * MOUNTED ON CHASSIS.
MAKE LINK A FOR REQD + VE VOLTAGE
MAKE LINK B FOR REQD - VE VOLTAGE

TELEGRAPH BATTERY

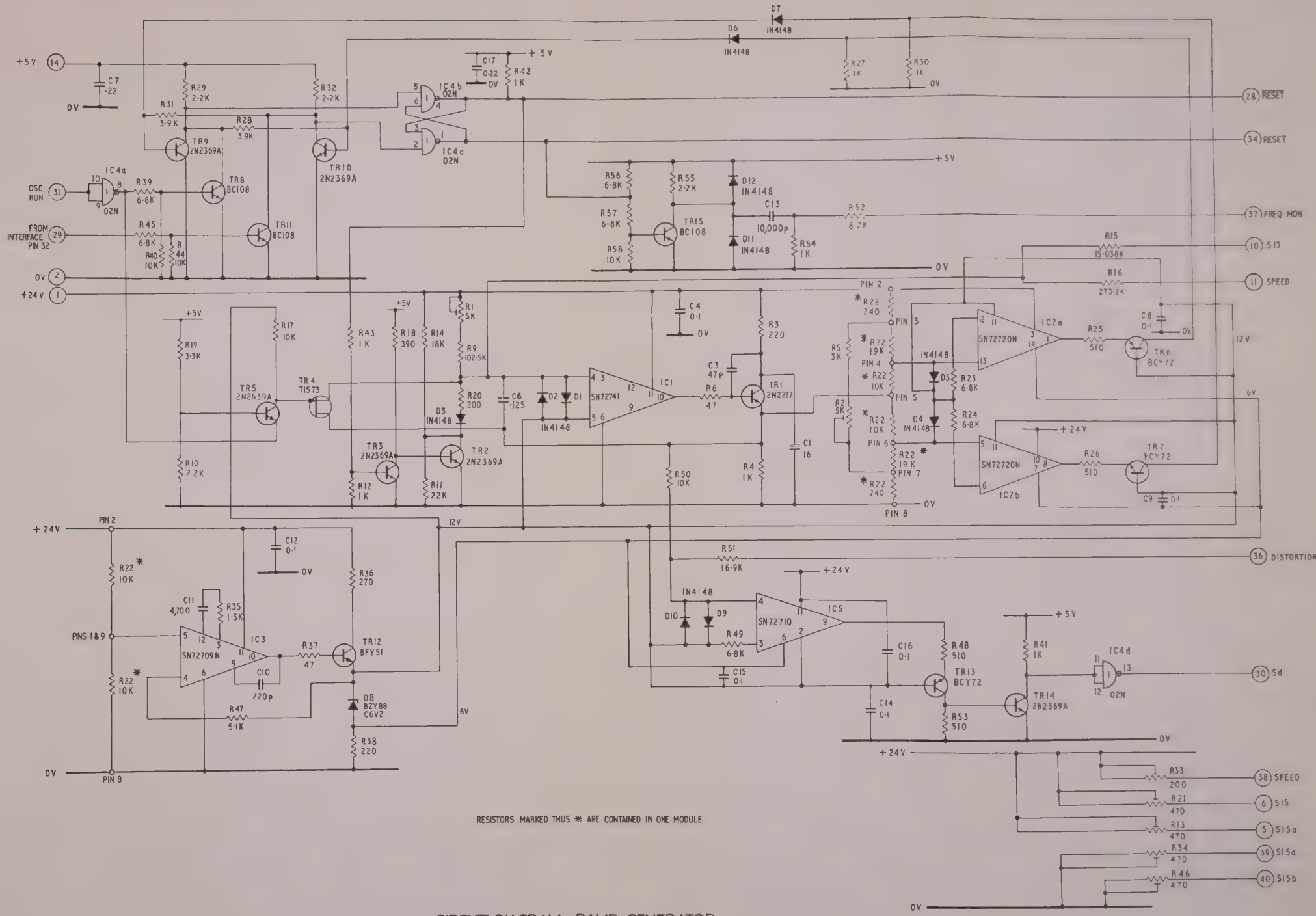
FIG. 8.7
TSG40.2




CIRCUIT DIAGRAM POWER SUPPLY

FIG. 8. 8.

620/DA/06347 ISS. 6

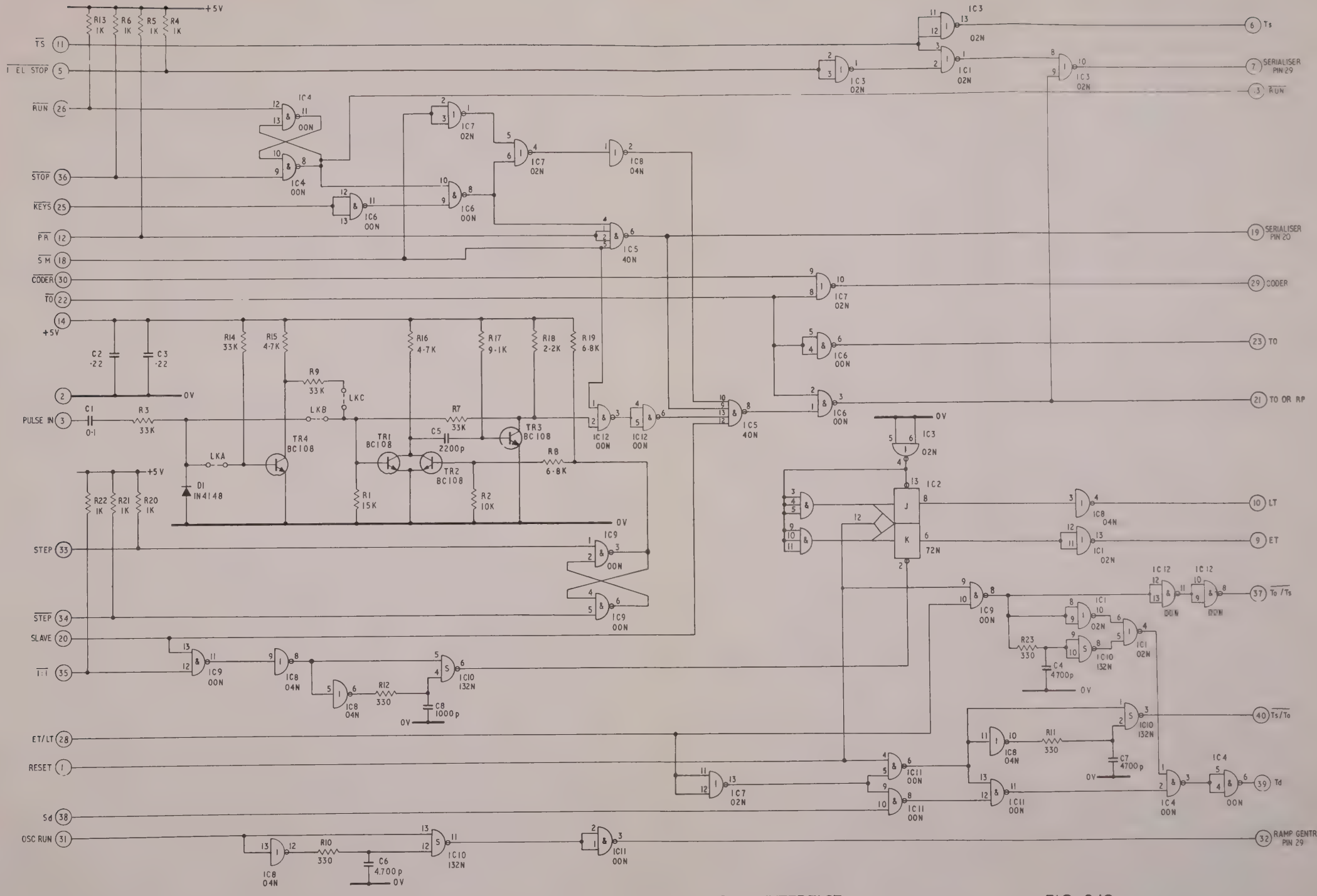



RESISTORS MARKED THUS * ARE CONTAINED IN ONE MODULE

CIRCUIT DIAGRAM - RAMP GENERATOR
DISTORTION GEN. & BAUDS MONITOR

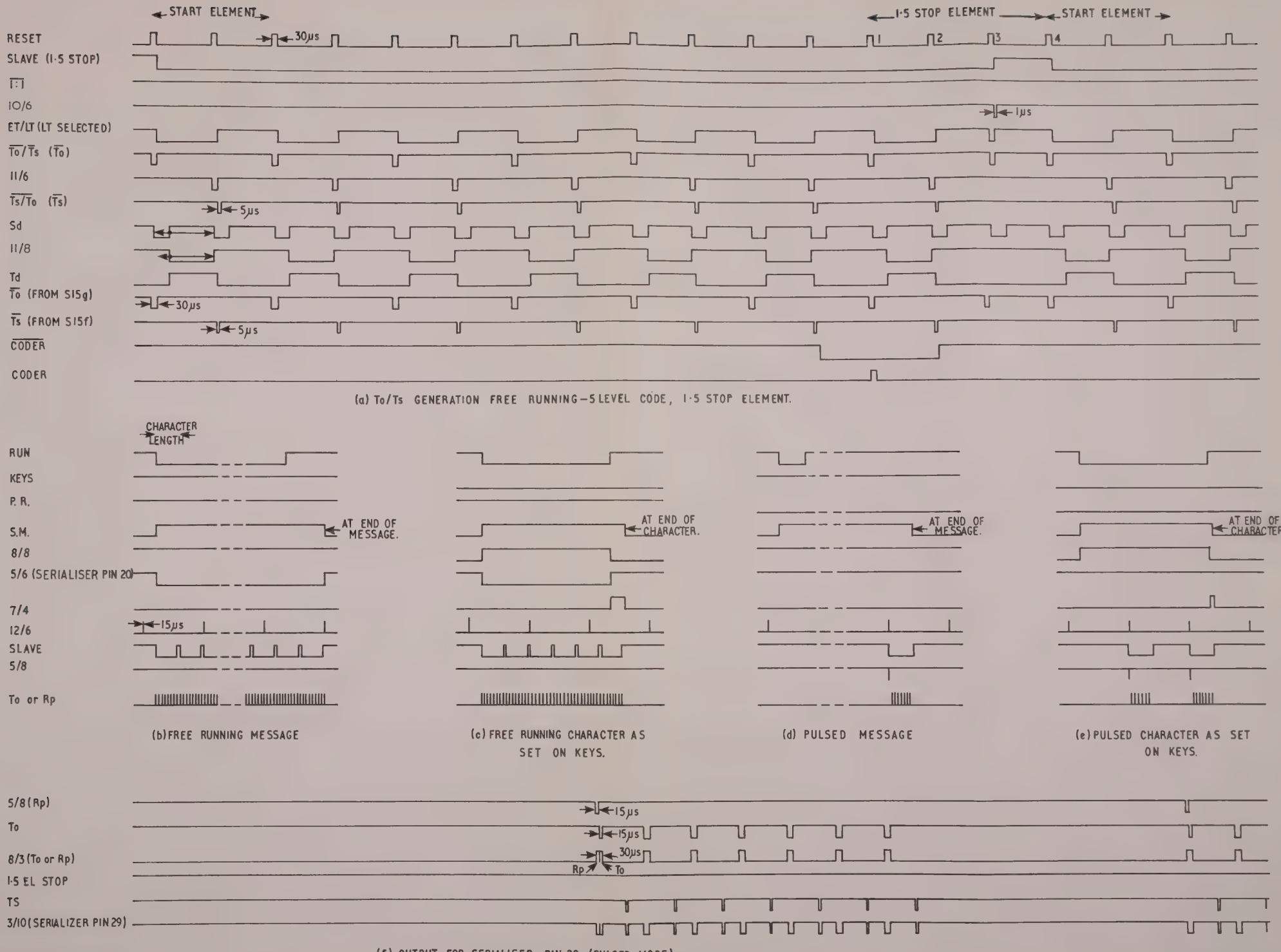
FIG. 8.9.

620/DA/06325 155.9




CIRCUIT DIAGRAM INTERFACE

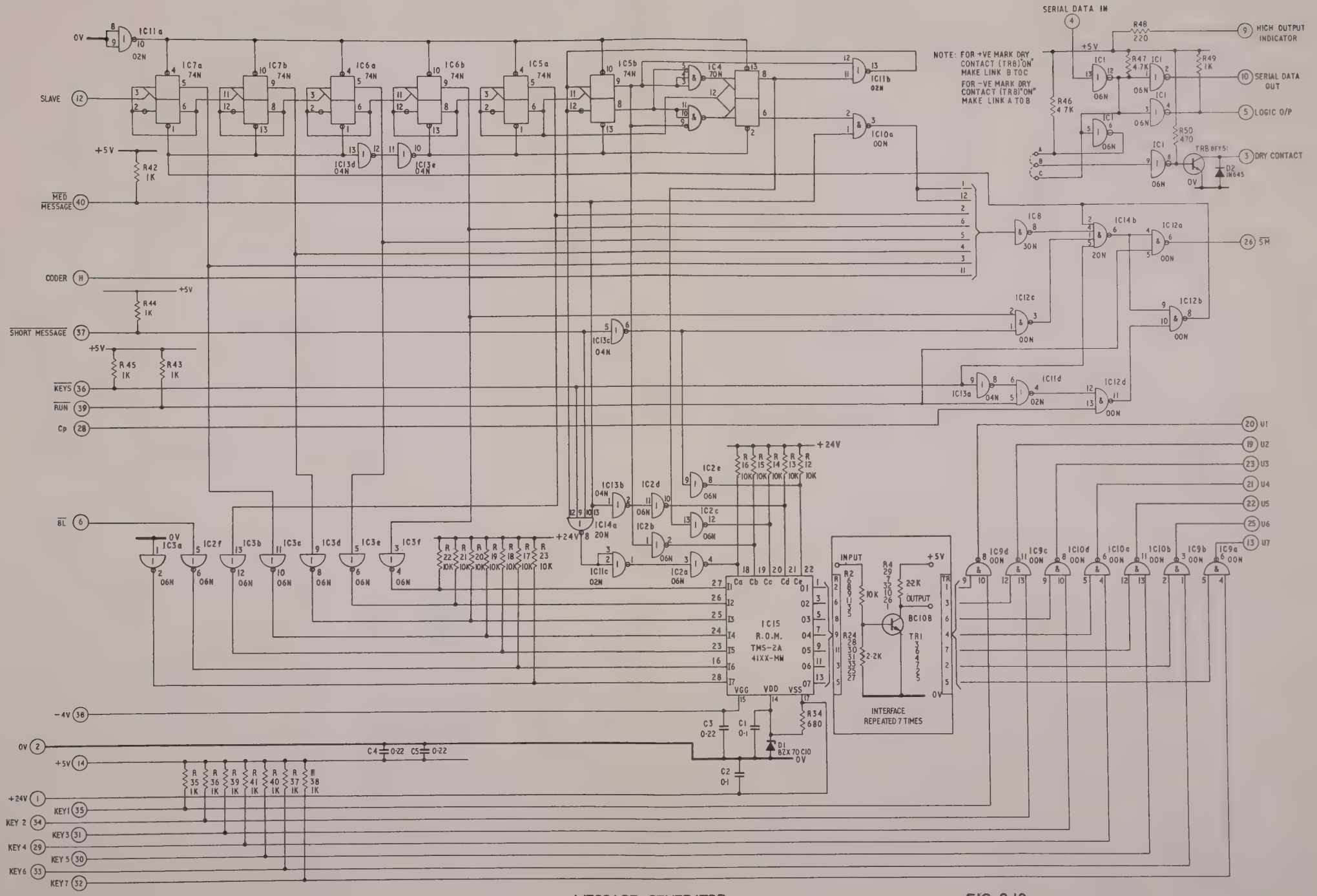
FIG. 8.10




620/DJ/0632OF
SHT. 11. ISS.1.

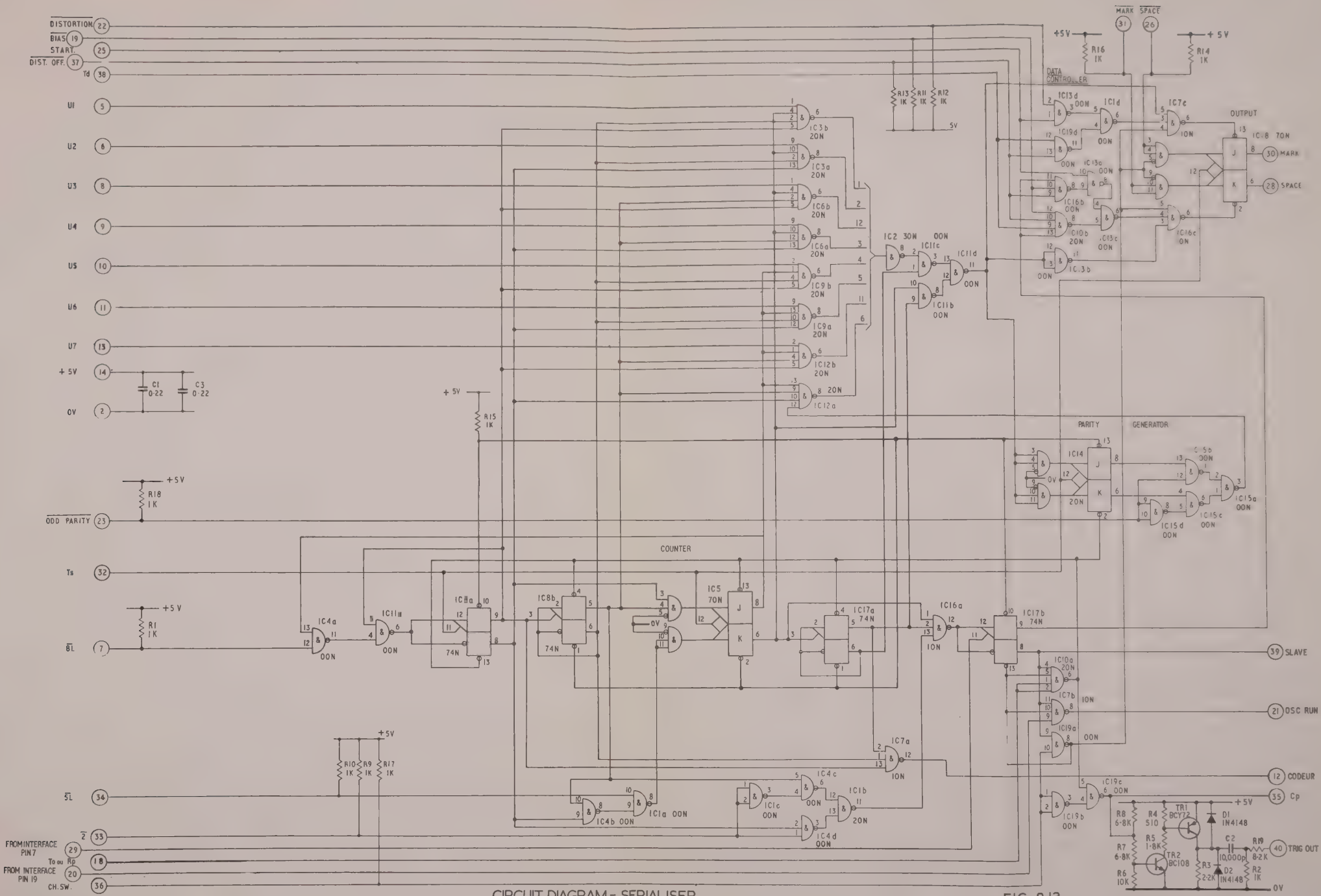
INTERFACE WAVEFORMS

FIG 8.11.



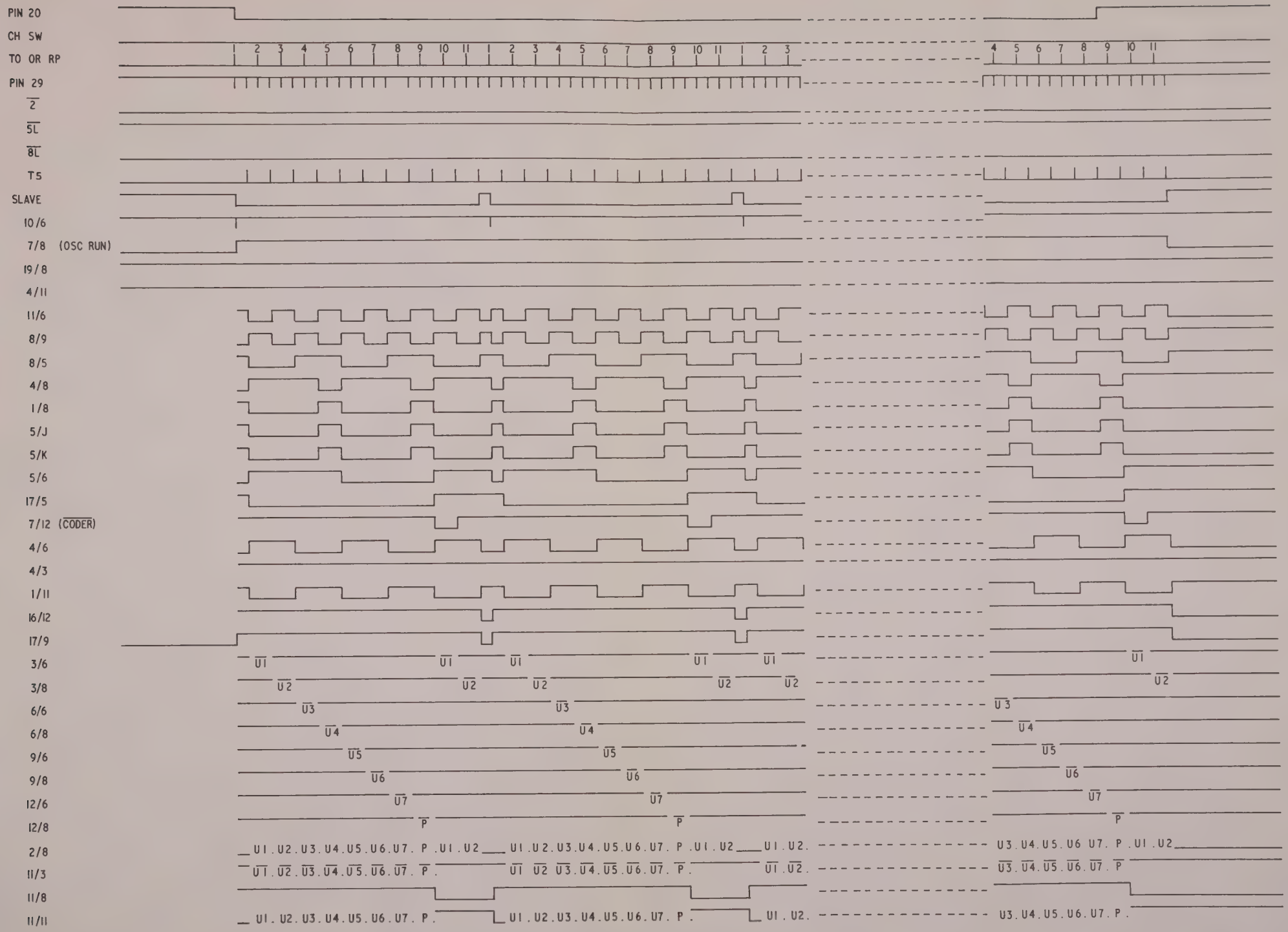

MESSAGE GENERATOR

FIG. 8.12




CIRCUIT DIAGRAM - SERIALISER

FIG. 8.13.

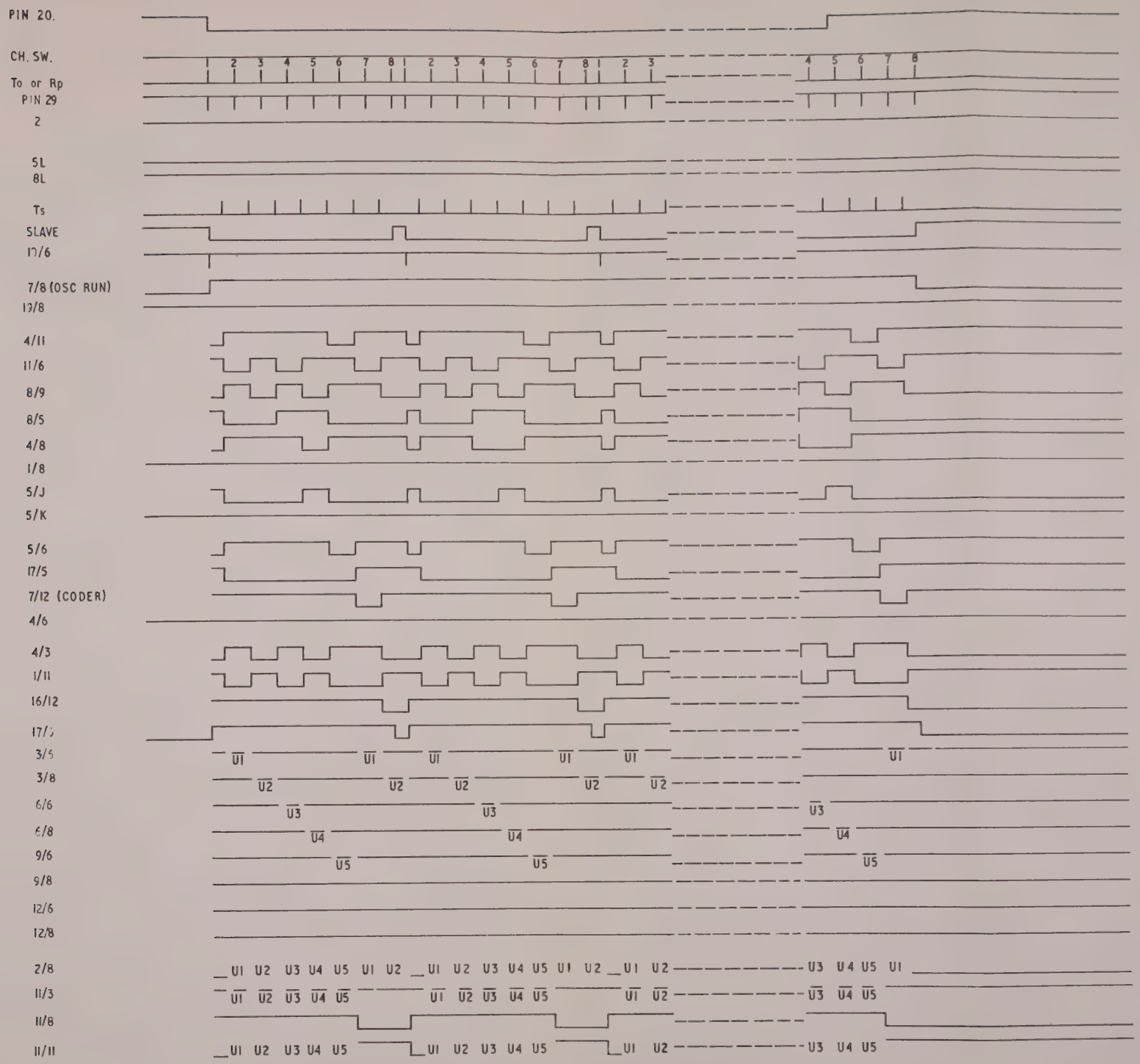



620/DJ/06320
SHT.12. ISS.2.

SERIALISER COUNTER AND MULTIPLEXER WAVEFORMS

FREE RUNNING WITH 8 LEVEL CODE AND 2 STOP ELEMENT

FIG 8.14

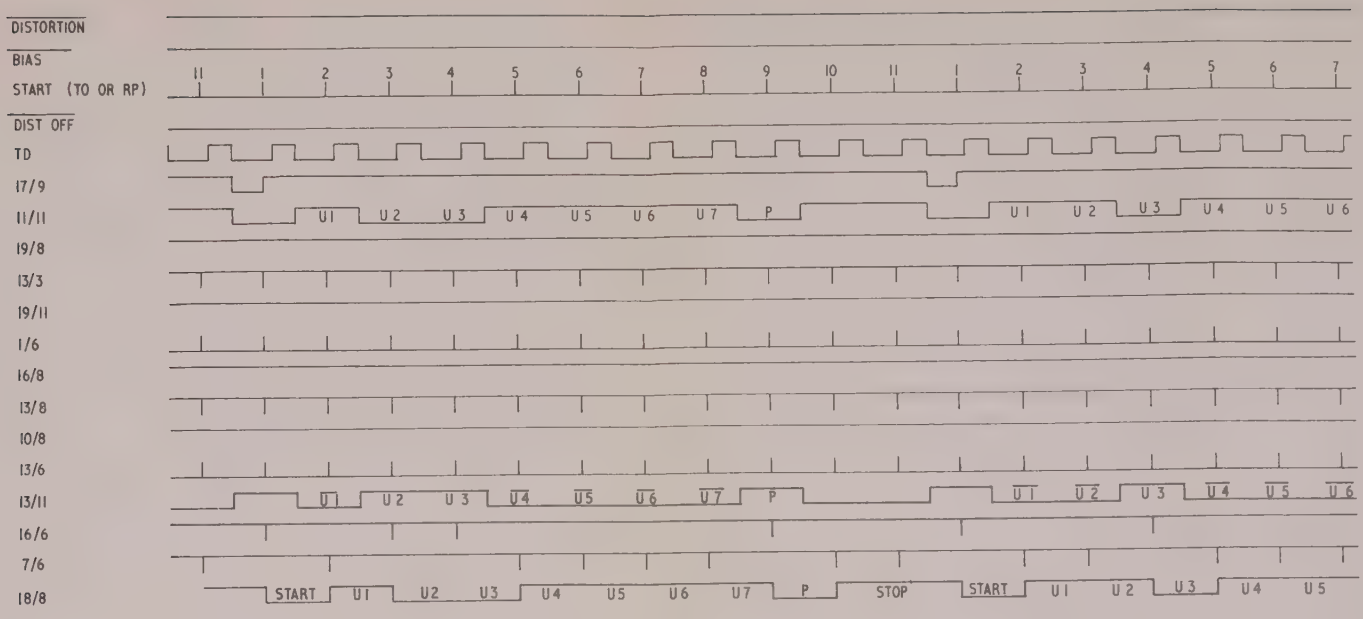



SERIALISER COUNTER AND MULTIPLEXER WAVEFORMS

FREE RUNNING WITH 5 LEVEL CODE AND 1·5 STOP ELEMENT.

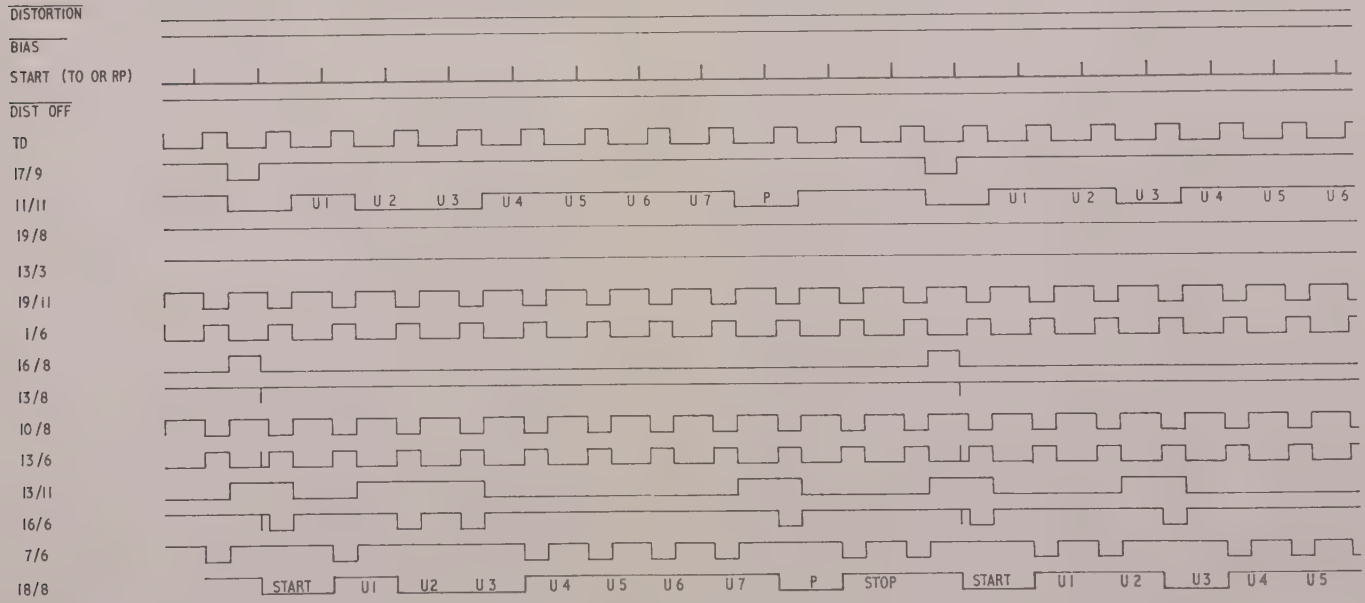
FIG. 8.15.

620/DJ/06320
SHT. 13. ISS 2




SWITCH SETTING :- STOP ELEMENT - 2, CODE 8 LEVEL
OUTPUT - CHARACTERS
DISTORTION - OFF
PARITY - ODD

(A)



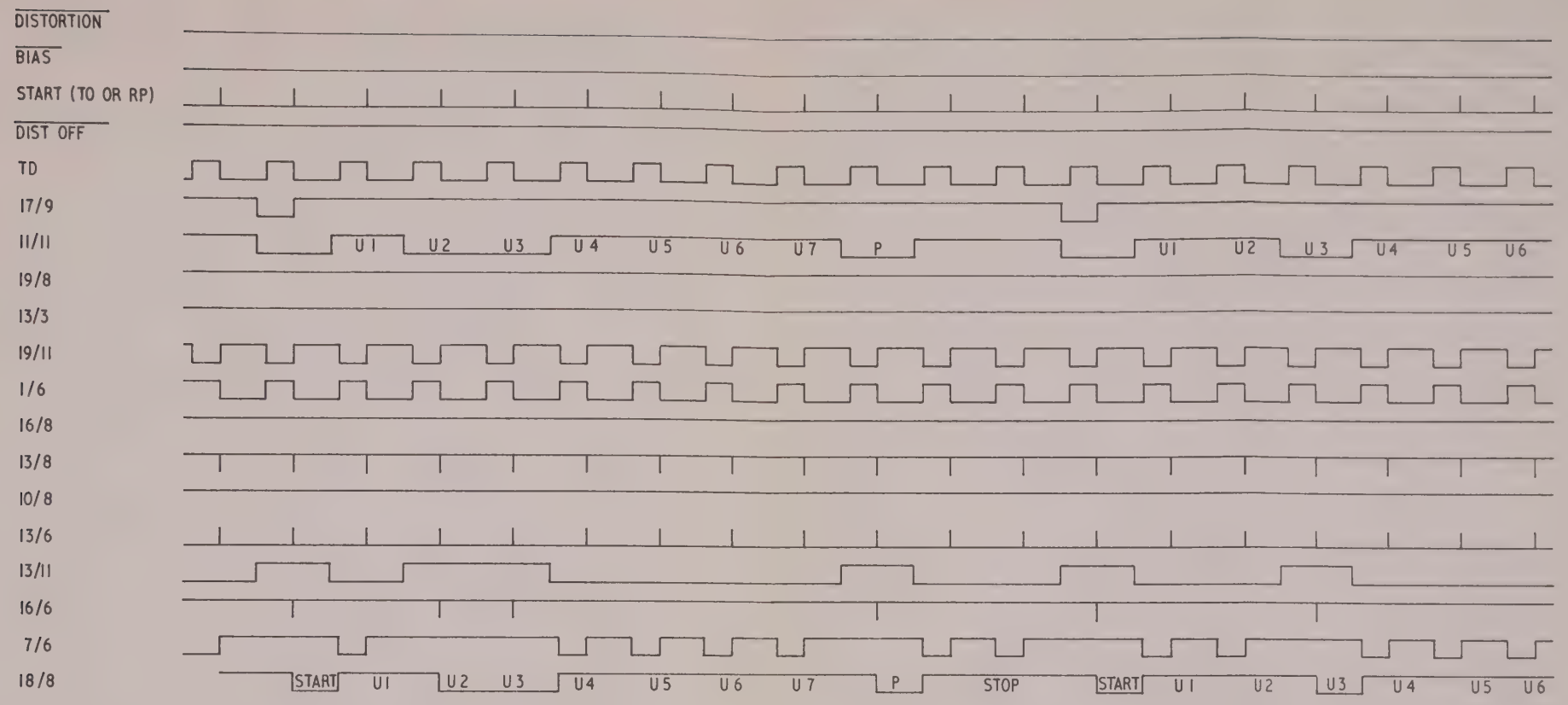

SWITCH SETTING :- STOP ELEMENT - 2, CODE 8 LEVEL
OUTPUT - CHARACTERS
DISTORTION - LONG START
PARITY - ODD

(B)

620/DJ/0632C
SHT 14 ISS 2

SERIALISER DATA CONTROLLER
AND OUTPUT WAVEFORMS.

FIG 8.16
SHEET 1

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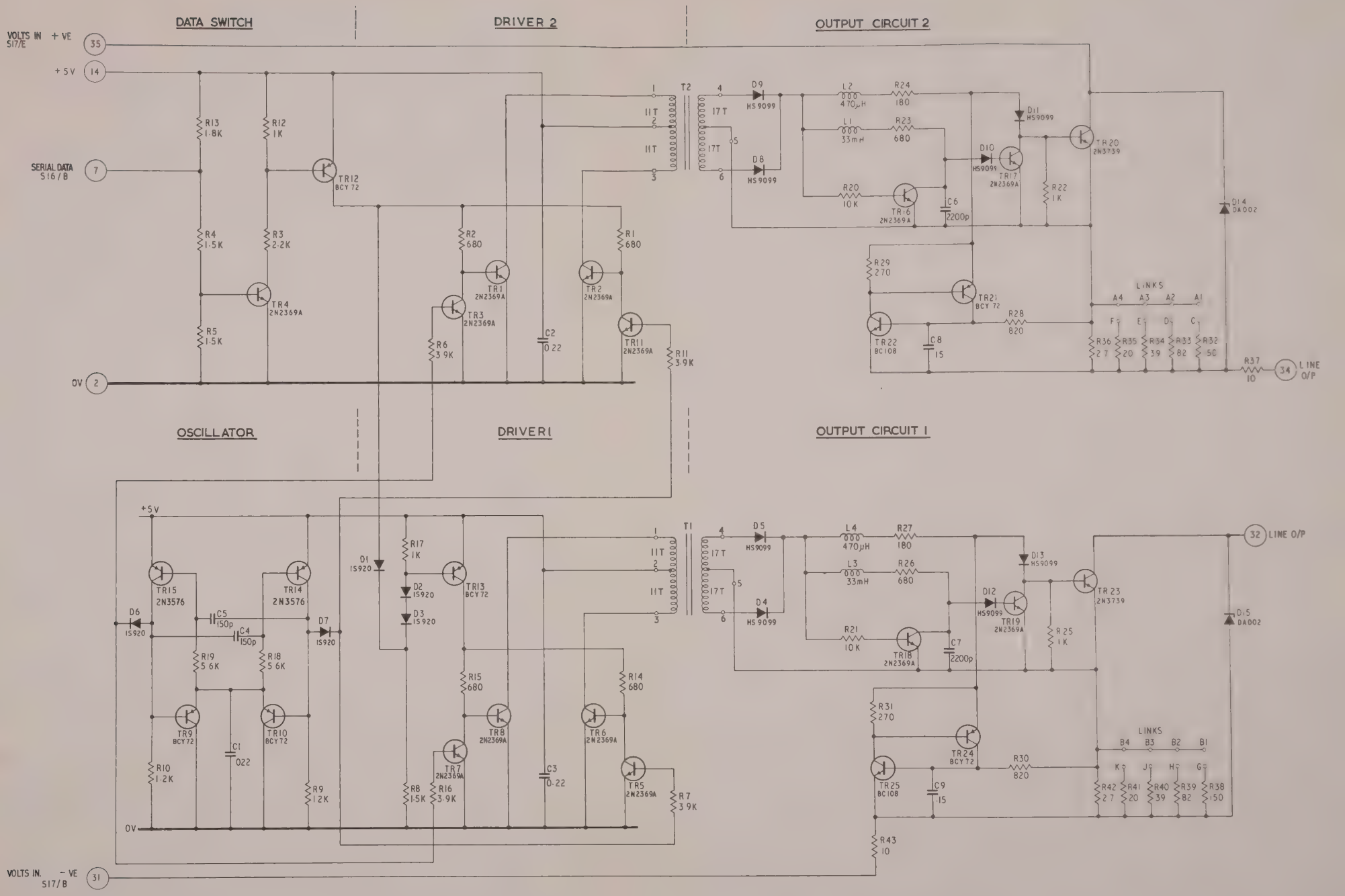
SHT.15.ISS.1.

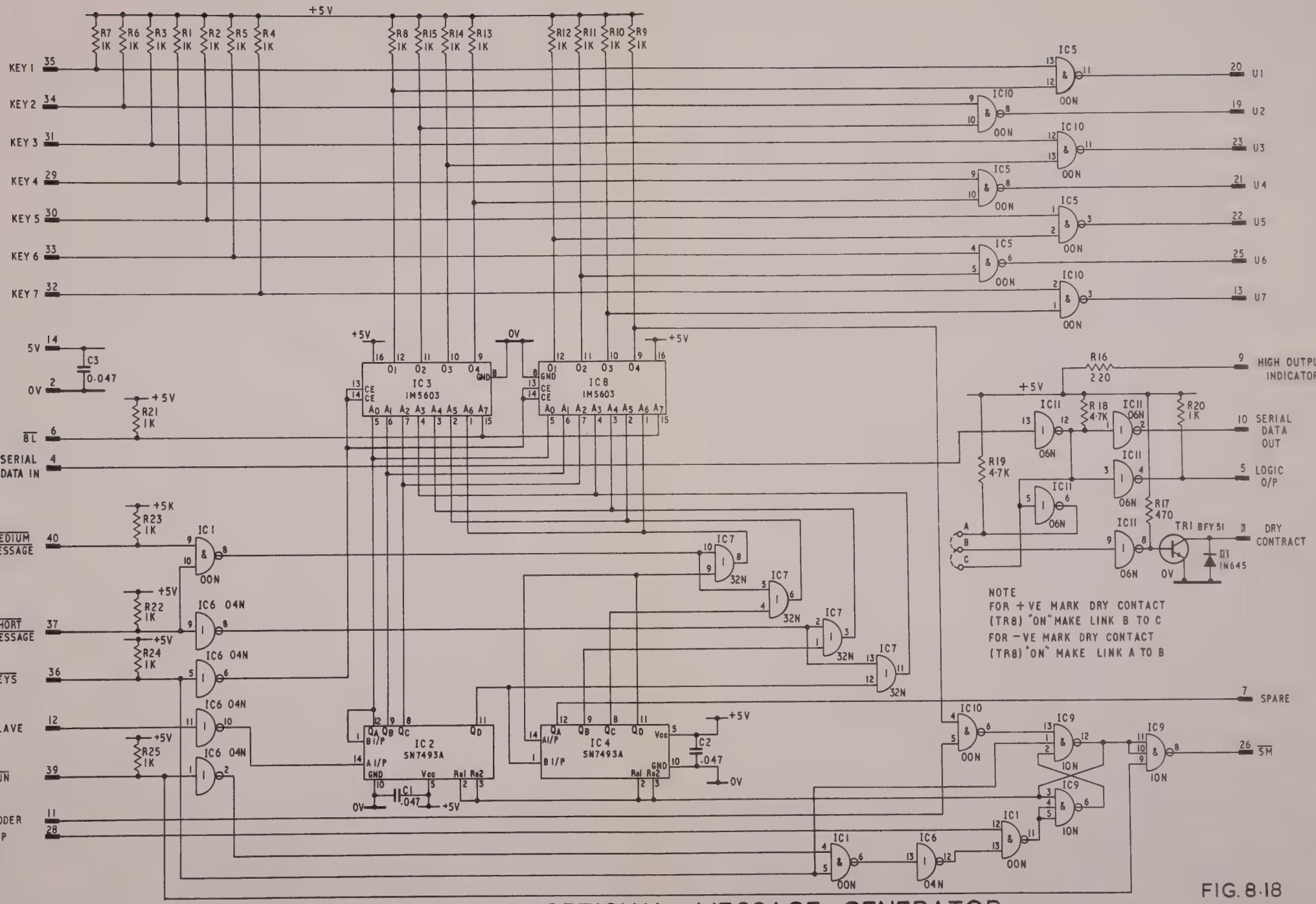
SERIALISER DATA CONTROLLER
AND OUTPUT WAVEFORMS

FIG 8.16
SHEET 2




CIRCUIT DIAGRAM - ELECTRONIC OUTPUT

FIG. 8.17




# OPTIONAL MESSAGE GENERATOR